

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte BASAVARAJ I. PAWATE and
BETTY PRINCE

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Appeal No. 96-1319
Application 07/934,982¹

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ON BRIEF
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Before URYNOWICZ, JERRY SMITH, and GROSS, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed August 25, 1992.

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-16, which constitute all the claims in the application. An amendment after final rejection was filed on May 18, 1995 and was entered by the examiner.

The disclosed invention pertains to a smart video memory for use in a method and apparatus for video processing. More particularly, the smart video memory has all the features of a conventional video memory as well as a processor for executing instructions on the same integrated circuit. The smart memory can operate in a standard mode in which the processor is not used or in a smart mode in which the processor handles some of the processing requirements of the video processing system.

Representative claim 1 is reproduced as follows:

1. A smart video memory, comprising:

data storage including a random access memory and a serial access memory;

a processor to execute instructions stored in said data storage and to read and write data in said data storage, said data storage and processor integrated in a single integrated circuit;

external leads coupled to said data storage and processor and extending from said single integrated circuit for externally connecting an external device to said data storage and processor, said external leads arranged such that the smart video memory is directly accessible as a standard video memory device by said external device while the processor is prevented from executing the instructions; and

at least one of said external leads comprising a serial data lead coupled to said serial access memory for serial data access.

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The examiner relies on the following references:

Nusinov et al. (Nusinov)	4,654,789	Mar. 31, 1987
Witt et al. (Witt)	4,731,737	Mar. 15, 1988

Nicoud, "Video RAMs: Structure and Applications," IEEE Micro, February 1988, pages 8-27.

Claims 1-16 stand rejected under 35 U.S.C. § 103. As evidence of obviousness the examiner offers Nicoud in view of Witt and Nusinov.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1, 4-7 and 9-16. We reach the opposite conclusion with respect to claims 2, 3 and 8. Accordingly, we affirm-in-part.

As a general proposition in an appeal involving a rejection under 35 U.S.C. § 103, an examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the briefs have not been considered [see 37 CFR § 1.192(a)].

With respect to independent claims 1, 11 and 16, the examiner cites Nicoud as teaching a smart memory in the form of a video RAM (VRAM). Nicoud does not teach that the “intelligence” of his smart memory comes from a processor integrated with the memory on a chip. Witt teaches a smart memory having a computer integrated with memory on a chip. Witt teaches that these smart memories are particularly advantageous in applications such as graphics. The examiner combines the teachings of Nicoud and Witt to obtain a smart VRAM which has memory and a processor on a single integrated circuit.

This combination does not suggest that the smart memory should operate in both a standard mode as well as the smart mode. Nusinov teaches integrated circuits having improved functionality which can operate as standard circuits (standard mode) with old devices, but can operate in enhanced modes (smart mode) with newer equipment. The examiner concludes that it would have been obvious to combine the collective teachings of Nicoud, Witt and Nusinov to arrive at the invention of the independent claims [answer, pages 3-4].

In our view, the examiner's analysis is sufficiently reasonable that we find that the examiner has satisfied the burden of presenting a prima facie case of obviousness. That is, the examiner's analysis, if left unrebutted, would be sufficient to support a rejection under 35 U.S.C. § 103. The burden is, therefore, upon appellants to come forward with evidence or arguments which persuasively rebut the examiner's prima facie case of obviousness. Appellants have presented several substantive arguments in response to the examiner's rejection. Therefore, we consider obviousness based upon the totality of the evidence and the relative persuasiveness of the arguments.

With respect to these independent claims, appellants argue that "none of these references disclose or suggest the external leads arranged so that the smart video memory is directly accessible as a standard memory device by the external device while

the processor is prevented from executing the instructions” [brief, pages 5-6]. We do not agree with this argument.

Nusinov discloses that an improved chip is designed to have an external pin which is unused for old or existing systems and is connected to external circuitry in new systems which can use the improved chip [column 1, lines 34-49]. Thus, Nusinov teaches that a new chip will appear as an old chip to existing systems but will appear as an enhanced chip to new systems. The collective teachings of Nicoud, Witt and Nusinov suggest a smart VRAM having a memory and computer on a chip which appears as a standard VRAM to existing equipment and as an enhanced VRAM or smart memory to new systems. The dual capability of this smart memory would be controlled by whether the normally unused external pin (such as pin 2 in Nusinov) is connected to an external signal indicating that the external system can use the enhanced features of the chip. When this smart memory is connected to an existing system, the unused external pin remains unconnected to the enhanced features of the chip. That is, the smart video memory of Nicoud, Witt and Nusinov would appear as a standard VRAM to existing equipment, and the enhanced feature of a computer on the chip would be prevented from executing instructions because it would remain disconnected from the external system. The operation of this enhanced circuit in an existing system fully meets the language of independent claims 1, 11 and 16. Thus, the collective teachings result in a smart memory

in which the computer is prevented from executing instructions because the computer is not connected to the existing equipment. This smart memory is directly accessible as a standard video memory in such existing equipment. Therefore, we sustain the rejection of the invention as broadly recited in independent claims 1, 11 and 16.

Claims 2 and 3 recite a smart memory having either an external lead or a memory location “for switching said processor between a smart mode and a standard mode.” Although the smart memory resulting from the collective teachings of Nicoud, Witt and Nusinov has a standard operating mode and a smart operating mode, the mode does not switch the on-chip processor in any manner. The collective teachings merely result in a smart memory in which the processor is connected or not connected through an external pin such as pin 2 of Nusinov. There is no suggestion that the processor itself has plural modes which are switchable in response to mode information. In our view, the connection or disconnection of the processor through external pin 2 does not teach or suggest a mode external lead or a mode information memory location for switching the processor between a smart mode and a standard mode. Therefore, we do not sustain the rejection of claims 2 and 3.

Claims 4 and 5 recite a smart memory having either an external lead or a memory location “for causing said processor to execute an interrupt task.” The smart memory resulting from the collective teachings of Nicoud, Witt and Nusinov would have a plurality of

external leads connected to external circuitry such as shown in Figure 3 of Witt. We agree with the examiner that the STAT 320 lead of Witt would have suggested the obviousness of an interrupt generate lead as broadly recited in claim 4. With respect to claim 5, we must determine the obviousness of maintaining information currently on an external lead within a predetermined memory location of the processor. We find this feature to be obvious as broadly recited in claim 5. The artisan would have appreciated and recognized the obviousness of maintaining status flag registers which indicate the current status of various ones of the external leads. Therefore, we sustain the rejection of claims 4 and 5.

Claims 6 and 7 recite a smart memory having either an external lead or a memory location “for resetting said processor.” As noted above, the smart memory resulting from the collective teachings of Nicoud, Witt and Nusinov would have a plurality of external leads connected to external circuitry such as shown in Figure 3 of Witt. We agree with the examiner that the RST 315 lead of Witt would have suggested the obviousness of a reset lead as broadly recited in claim 6. With respect to claim 7, we again note that the artisan would have appreciated and recognized the obviousness of maintaining status flag registers which indicate the current status of various ones of the external leads. Therefore, we sustain the rejection of claims 6 and 7.

Claim 8 recites a smart memory having a memory location “for causing said processor to start and stop executing instructions.” Although the smart memory resulting

from the collective teachings of Nicoud, Witt and Nusinov has a standard operating mode and a smart operating mode, the mode determination does not modify the on-chip processor in any manner as noted above. The collective teachings merely result in a smart memory in which the processor is connected or not connected through an external pin such as pin 2 of Nusinov. There is no suggestion that the processor itself can be directed to start and stop executing instructions in response to an external lead or a predetermined location in the processor memory. In our view, the connection or disconnection of the processor through external pin 2 does not teach or suggest a memory location for causing the processor to start and stop executing instructions. Therefore, we do not sustain the rejection of claim 8.

Claims 9 and 10 recite a smart memory having either an external lead or a memory location “for indicating completion of a task by said processor.” As noted above, the smart memory resulting from the collective teachings of Nicoud, Witt and Nusinov would have a plurality of external leads connected to external circuitry such as shown in Figure 3 of Witt. We agree with the examiner that the DONE 321 lead of Witt would have suggested the obviousness of a task completed lead as broadly recited in claim 9. With respect to claim 10, we again note that the artisan would have appreciated and recognized the obviousness of maintaining status flag registers which indicate the current status of various ones of the external leads. Therefore, we sustain the rejection of claims 9 and 10.

Claim 12 recites a system in which the central processing unit “offloads a task to said integrated circuit to be executed by said processor.” Witt specifically discloses that the advantage of a smart memory is that tasks can be offloaded from the host system computer to the smart memory processors [column 2, lines 49-52]. Therefore, we sustain the rejection of the invention as broadly recited in claim 12.

Claim 13 recites a system in which the processor “is halted during accesses to said integrated circuit.” The examiner views this halting operation as equivalent to the prevention of the processor from executing as recited in the independent claims [answer, page 12]. Appellants traverse this position for the same reasons discussed with respect to the independent claims [reply brief, page 5].

As we noted above with respect to claims 1, 11 and 16, the processor of the smart memory resulting from the teachings of Nicoud, Witt and Nusinov would not be connected at all when it is inserted into an existing system where the unused external lead remains disconnected. Thus, the processor is not operational, or is halted, during external accesses from such an existing system. We also observe that the artisan familiar with the operation of computers would have found it obvious to broadly halt the operation of a device when a higher priority request is made for the device. Since access of the smart device from an external host system is clearly more important than its internal processing, we sustain the rejection of the invention as broadly recited in claim 13.

Claim 15 recites a system which has a bus arbitrator, a bus request external lead and a bus grant external lead. The examiner observes that Nicoud discloses bus arbitration [answer, page 12]. Appellants argue that the mere disclosure of bus arbitration does not disclose or suggest the specific functions of claim 15 [reply brief, page 5].

We agree with the position of the examiner. There are no specific functions recited in claim 15. Instead, claim 15 merely recites that the external leads of the integrated circuit include a bus request lead and a bus grant lead for controlling a bus arbitrator. The artisan familiar with the computer arts would have understood that bus arbitration in computers was conventional whenever there is contention for use of a bus. Since the smart memory resulting from the teachings of Nicoud, Witt and Nusinov is connected to a host external processor, it would have been obvious to one having ordinary skill in the art to provide leads for the external processor to take control of the system bus of the smart memory. Therefore, we sustain the rejection of claim 15.

In summary, we have sustained the examiner's rejection of claims 1, 4-7 and 9-16, but we have not sustained the examiner's rejection of claims 2, 3 and 8. Accordingly, the decision of the examiner rejecting claims 1-16 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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Stanley M. Urynowicz, Jr.
Administrative Patent Judge

Jerry Smith
Administrative Patent Judge

Anita Pellman Gross
Administrative Patent Judge

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