

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL L. ZIEGLER, ROBERT J. BROOKS, WILLIAM R. BRYG,
CRAIG R. FRINK, THOMAS R. HOTCHKISS, ROBERT D. ODINEAL,
JAMES B. WILLIAMS and JOHN L. WOOD

Appeal No. 1996-1259
Application 08/201,185¹

ON BRIEF

Before BARRETT, FLEMING, and FRAHM, Administrative Patent Judges.

FRAHM, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 4, which constitute all of the

¹ Application for patent filed February 24, 1994.

pending claims in the application before us.

BACKGROUND

The subject matter on appeal is directed to a data processing system that has a shared bus, and to controlling transactions issued on the shared bus using coherency checks (see specification, pages 1 and 2). Appellants admit in the specification that shared buses are conventional (see specification, page 3), and that coherency checking schemes are known in the prior art (see specification, page 2). Appellants recognized that a known problem in the prior art was that coherency checking can be slow due to complex handshaking requirements and multiple transactions such as busy/abort signals (see specification, pages 3 to 5). Appellants' have attempted to overcome these drawbacks with the prior art by providing a transaction queue in each client module connected to the bus, and a bus controller, separate from the client modules, which limits transactions on the bus when a queue in one of the modules has less than a certain amount of free space (see specification, page 5).

Representative independent claim 1 is reproduced below:

1. A data processing system comprising:

a bus having a plurality of signal conductors for transmitting information between physically separated locations;

a plurality of modules coupled to said bus, each said module comprising means for transmitting and receiving information specifying a transaction to be carried out by another module or by said module, respectively, each said module further comprising a queue for storing information specifying said transaction received by said module for processing by said module;

a bus controller, separate from said modules for generating a signal on said bus indicative of the types of said transactions that can be sent on said bus by said modules;

means, separate from said modules, for determining that a queue in one of said modules has less than a predetermined amount of free space and for causing said bus controller to limit transactions that can be sent on said bus so as to prevent transactions requiring space in said queue from being issued.

Representative dependent claim 4 is reproduced below:

4. The data processing system of Claim 1 further comprising a main memory, said main memory including a queue for storing instructions requiring responses by said main memory, and wherein said determining means further comprises:

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a buffer having one location for each slot in each said queue in said modules storing coherent transaction information.

The following reference is relied on by the examiner:

Sindhu et al. (Sindhu)	5,265,235	Nov. 23,
1993		

Claims 1 to 4 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Sindhu alone.

Rather than repeat the positions of appellants and the examiner, reference is made to the Briefs and the Answer for the respective details thereof.²

OPINION

At the outset, we note our agreement with appellants (Brief, page 3) that claims 1 to 3 should stand or fall together as a first group, and that dependent claim 4 should also stand separately as a second group. We will take sole

²We note that the after final amendment of May 12, 1995, has been entered as per the Advisory Action of May 31, 1995. We also note that the power of attorney of August 7, 1995, has been entered as per the petition decision of September 20, 1995.

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independent claim 1 as being representative of the first group, and claim 4 as being representative of the second group.

In reaching our conclusion on the issues raised in this appeal, we have carefully considered appellants' specification and claims, the applied reference, appellants' admitted prior art, and the respective viewpoints of appellants and the examiner. We note that we have only considered those arguments

made by appellants, and that any arguments not presented by appellants are considered waived and have not been considered. 37 CFR § 1.192(a)(1995).

As a consequence of our review, we are in general agreement with the examiner (Answer, pages 2 to 5) that the prior art of Sindhu would have fairly taught or suggested the invention of claims 1 to 3 on appeal. However, because we agree with appellants (Brief, pages 3 to 4) that the applied prior art fails to teach or suggest the recited details of the

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main memory, instruction queue, and coherent transaction buffer, we cannot sustain the rejection of claim 4 on appeal. For the reasons which follow, we will sustain the decision of the examiner rejecting claims 1 to 3 under 35 U.S.C. § 103, and we will reverse the decision of the examiner rejecting claim 4 under 35 U.S.C. § 103.

Rejection of Claims 1 to 3 Under 35 U.S.C. § 103:

Turning first to the rejection of claims 1 to 3 under § 103, we find that claims 1 to 3 on appeal would have been obvious to one of ordinary skill in the art at the time the invention was made in light of the teachings of Sindhu, especially to the extent the invention is broadly set forth in representative claim 1.

We find that Sindhu would have fairly taught or suggested all of appellants' broadly recited features of claim 1 of a data processing system (Figure 1) having a bus (global bus 26), a plurality of modules (14a, 14b, 14i), a bus controller (arbiter 36 and/or controller 25), and means for determining the amount of module queue free space which is "separate from said modules" (arbiter 36 and/or controller 25; column 9,

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lines 29 to 51). Sindhu discloses that bus 26 is "independently arbitrated by arbiters 35a, 35b, 35i, and 36" (column 6, lines 16 to 17), and that "[t]he arbiters 35a-35i and 36 . . . ensur[e] that each client has fair, bounded time access to its host bus" (column 7, lines 44 to 48). Because at least one of Sindhu's arbiters, arbiter 36, is "separate from" the client modules 14a-i, we find that Sindhu reads on appellants' broad claim 1 on appeal, to the extent that representative claim 1 does not require that overflow detection not also be performed by the client modules (i.e., decentralization).

We agree generally with the examiner (Answer, page 2) that the ordinarily skilled artisan looking at the teachings and suggestions of Sindhu would have found it obvious to monitor the transaction queues of the individual client modules from a central location (36 and/or 25) separate from the modules (14a-i). While we note that there is no per se rule as to the obviousness of shifting location of parts such as suggested by the examiner's reliance upon In re Japikse, 86 USPQ 70, 73 (CCPA 1950), we do find that it would have been

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obvious to perform queue monitoring "separate from" the modules 14a-i in light of Sindhu's provision of a separate bus arbiter 36 and separate bus controller 25. As just discussed above, individual arbiters 35a-i as well as arbiter 36 act to control overflow detection. And, more importantly, we find that claim 1 on appeal does not specifically require that the overflow detection function/hardware not be in the client modules, or that the overflow detection function/hardware be only be present in the means for determining. Appellants' claim 1 on appeal does not require the presence of another queue such as the disclosed scoreboard 178.

We cannot agree with appellants' argument (Brief, page 3) that claims 1 to 3 are non-obvious because the queue overflow detection function has been duplicated and not just moved. Although appellants assert that in order to function in a central location the overflow system must duplicate the modules' contents, we note find that representative claim 1 does not require queue content duplication. We find that only claim 4 on appeal requires queue content duplication. Broadly set forth claim 1 on appeal merely calls for a bus controller

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and a means for determining (i.e., overflow detection) as being "separate from said modules," and does not require that the hardware be duplicated in the client modules and the means for determining. We agree with the examiner (Answer, pages 2 and 4) that the present invention of claim 1 on appeal is not specifically drawn toward or limited to centralization and that no specific details exist in the claims which relate to centralization as opposed to decentralization of overflow detection.

With respect to dependent claims 2 and 3, appellants have not made any separate arguments as to these claims. Since appellants present no separate arguments as to claims 2 and 3, these claims fall with parent claim 1, discussed supra.

Rejection of Claim 4 Under 35 U.S.C. § 103:

We turn next to the question of the obviousness of claim 4 under § 103. Dependent claim 4 on appeal recites the details of a main (i.e., centralized) memory having its own instruction queue as well as a buffer for storing coherent transaction information. Appellants argue (Brief, page 3) that this duplicate hardware (the instruction queue and

buffers) is not

discussed or suggested by Sindhu. We agree. The main memory instruction queue and determining means coherent transaction buffer operate in concert together to achieve an important aspect of appellants' invention of providing a system that handles multiple transactions without imposing unnecessary delays or design complexity. We find that the applied prior art fails to teach or suggest such a main memory having an instruction queue and a determining means having a coherent transaction buffer. We find that the main memory of claim 4 is neither taught nor suggested by the applied reference to Sindhu, and accordingly we cannot sustain the examiner's rejection under 35 U.S.C. § 103 as to claim 4.

In light of the foregoing, the differences between the subject matter recited in claims 1 to 3 and the prior art are such that the claimed subject matter as a whole would have been obvious within the meaning of 35 U.S.C. § 103. Accordingly, we shall sustain the standing rejections of claims 1 to 3. We reach the opposite conclusion with respect

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to claim 4 which recite the details of the means for determining having a queue and buffer.

CONCLUSION

The decision of the examiner rejecting claims 1 to 3 under 35 U.S.C. § 103 is affirmed.

The decision of the examiner rejecting claim 4 under 35 U.S.C. § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

LEE E. BARRETT)
Administrative Patent Judge)
)
)
) BOARD OF PATENT
MICHAEL R. FLEMING)
Administrative Patent Judge) APPEALS AND
)
) INTERFERENCES

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