

**THIS OPINION WAS NOT WRITTEN FOR PUBLICATION**

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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***Ex parte*** HIROYUKI FUKUYAMA

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Appeal No. 96-1247  
Application 08/115,662<sup>1</sup>

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HEARD: August 5, 1999

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Before KRASS, FLEMING and FRAHM, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge.***

**DECISION ON APPEAL**

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<sup>1</sup> Application for patent filed September 3, 1993.

This is a decision on appeal from the final rejection of claims 1 through 4, 6 through 9, 13, 14 and 17. Claim 5 has been objected to by the Examiner. Claims 10 through 12, 15, 16 and 18 have been cancelled. Thus, claims 1 through 9, 13, 14 and 17 are pending in the application.

This invention relates to clock feeding circuitry in an integrated circuit and a method for adjusting clock skew in such integrated circuits. On page 7 of the specification, Appellant discloses that Figure 1 shows a semi-custom-made LSI, using a clock feeding circuitry according to a preferred embodiment of the invention. Appellant further discloses that Figure 1 shows that the semi-custom-made LSI has a module structure of logic circuits. The modules have user-designed regions 130, 150 and 170. On pages 7 and 8 of the specification, Appellant discloses that within each region the interconnections for feeding the clock signals to the logic circuits are provided so as to minimize the clock skew between the logic circuits in the region. Appellant further discloses that adjustable delay devices 152 and 172 are used to adjust

the clock skew between the clock input 103 and the input to each region 151 and 171, respectively. Independent claim 1 is reproduced as follows:

1. An integrated circuit formed as a semi-custom-made LSI device having a conductive pattern, the integrated circuit comprising:

having a plurality of logic circuit regions, each region

a plurality of logic circuits,

and an input circuit for receiving a clock signal providing the received clock signal to each of said plurality of logic circuits, and

pattern, interconnections formed by the conductive the interconnections electrically connecting said plurality of logic circuits and said input circuit, so that a clock skew of the clock signal is minimized among said plurality of logic circuits;

a clock source for feeding said clock signal to said regions; and

a plurality of adjusting circuits, each adjusting circuit disposed between said clock source and a respective one of said regions, each adjusting circuit delaying transmission of the clock signal to the respective region, said each adjusting circuit including a predetermined number of delay elements selectively connected between said clock source and the respective one of said regions with the conductive pattern so as to adjust the amount of the delay of the clock signal.

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The Examiner relies on the following references:

Johnson et al. (Johnson)	5,077,676	Dec. 31, 1991
Deyhimy et al. (Deyhimy)	5,204,559	Apr. 20, 1993

Claims 1 through 4, 6 through 8, 14 and 17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Deyhimy. Claims 9 and 13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Deyhimy in view of Johnson.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the briefs<sup>2</sup> and answer for the respective details thereof.

#### **OPINION**

We will not sustain the rejection of claims 1 through 4, 6 through 9, 13, 14 and 17 under 35 U.S.C. § 103.

The Examiner has failed to set forth a **prima facie** case. It is the burden of the Examiner to establish why one

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<sup>2</sup> Appellant filed an appeal brief on July 24, 1995. Appellant filed a reply brief on October 10, 1995. The Examiner stated in a letter mailed January 16, 1996 that the reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

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having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d

1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assoc., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

Claims 1 through 4, 6 through 8, 14 and 17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Deyhimy. On page 3 of the Examiner's answer, the Examiner argues that Deyhimy shows in Figure 3 all the structure set forth in independent claims 1 and 14 except for the fact that

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Deyhimy does not teach using equal signal links between the adjusting circuits and the logic circuits. The Examiner states that this design is notoriously well known.

Appellant argues on page 7 of the brief that independent claim 1 is directed to an integrated circuit which comprises "a plurality of logic circuit regions" where each logic circuit region has "interconnections" which are formed by a conductive pattern "so that a clock skew of the clock signal is minimized among" logic circuits in the logic circuit region. Appellant also points out that claim 1 also specifies "a plurality of adjusting circuits" between a clock source and the logic circuit region in order to adjust the amount of delay of the clock signal. Appellant points out that claim 1 thus provides for clock skew minimization at two levels, at the logic circuit region level and at the clock source to the logic circuit region level. Appellant argues that there is nothing in Deyhimy that would give an incentive to an ordinary skilled person to mount such a multi-level attack on clock skew.

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On page 8 of the brief, Appellant argues that independent claim 14 is directed to an integrated circuit which comprises first and second logic circuit regions and first and second adjusting circuit regions which are coupled between input buffer circuits and input terminals of the logic circuit region. Appellant points out that independent claim 14 specifies that the first adjusting circuit has "an input, an output and a predetermined number of delay elements, a number of the delay elements being selected . . . and being connected between the input and output of said first adjusting circuit with a conductive pattern." Appellant further points out that independent claim 1 also claims a second adjusting circuit that is similar. Appellant argues that Deyhimy does not suggest or disclose using a conductive pattern to connect a number of delay elements selected from a predetermined number of delay elements that are available. Furthermore, we note that independent claim 14 also claims "a first logic circuit region having . . .

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a plurality of first logic circuits coupled to the output of the first buffer, each of the first logic circuits receiving the clock signal with a first delay time." We further note that the same language is provided for a second logic circuit region. Therefore, independent claim 14 also requires a conductive pattern for the first logic circuits that will provide a clock skew of the clock signal that is minimized. Appellant argues that Deyhimy fails to teach or suggest using a conductive pattern to connect a number of delay elements which provides local and global levels of clock skew minimization.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

Turning to Deyhimy, we agree with the Examiner that Deyhimy's Figure 3 only shows skew adjusting circuits 122-1

through 122-N and fails to show that the interconnections in the regions that these adjusting circuits provide are designed such

as to minimize skew. Turning to column 2 of Deyhimy, we find that Deyhimy states that the variable delay elements 120 and 122 are added to the clock distribution circuit as a prior art known method of eliminating skew between clock outputs.

Deyhimy discloses that the components of the computer system have been assembled onto a printed circuit board and that the delay elements 120 and 122 are adjusted to add delay so that the skew between the master clock output 104 is nearly eliminated. Deyhimy further discloses in column 2, lines 36-41, that Figure 3's conventional adjustment procedure is very time consuming and is also prone to inaccuracy. Deyhimy does not teach or suggest that Figure 3 adjusts the skew or eliminates the skew by designing the printed circuit boards such that skew is minimized in the circuit board region. In fact, Deyhimy does not seek this solution to the problem. Deyhimy's invention is directed to adjusting the clock

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skew on an ongoing basis. Deyhimy discloses in column 2, line 61, through column 3, line 15, that the preferred embodiment of their invention is to provide delay blocks. The delay elements are switched into or out of the master clock output path in a binary-weighted group, thereby minimizing the required number of switching means

necessary to obtain any desired delay. The skew between each of the master clock signals can be measured and the switching means can be employed to reduce the skew to a minimum. Thus, Deyhimy solves the skew problem, not by designing the PC circuit boards such that the interconnections minimize skew but instead by measuring the skew on an ongoing basis and switching in or out delay elements on an ongoing basis to counteract the skew. Thus, Deyhimy does not provide any suggestion, incentive or reason to one of ordinary skill in the art to provide connections at the circuit board such that skew is minimized between logic elements as claimed by Appellant's independent claims 1 and 14. Therefore, we will not sustain the Examiner's rejection of claims 1 through

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4, 6 through 8, 14 and 17 under 35 U.S.C. § 103 as being unpatentable over Deyhimy.

Claims 9 and 13 are rejected under 35 U.S.C. § 103 as being unpatentable over Deyhimy in view of Johnson. We note that independent claim 9 recites "simulating a first hypothetical interconnection between the plurality of logic circuits in each logic circuit region so that the clock skew of the clock signal is minimized among the logic circuits of each logic circuit region." We also note that independent claim 13 recites "determining a layout and interconnections of each logic circuit

region by which a clock skew of the clock signal transmitted from the clock source to the logic circuit regions is minimized among the logic circuits of each logic circuit region." We further note that the Examiner relies on Deyhimy as above to meet these limitations. Therefore, we will not sustain the rejection of claims 9 and 13 under 35 U.S.C. § 103 as being unpatentable over Deyhimy in view of Johnson for the same reasons as we pointed out above.

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We have not sustained the rejection of claims 1 through 4, 6 through 9, 13, 14 and 17 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

**REVERSED**

	ERROL A. KRASS	)	
	Administrative Patent Judge	)	
		)	
		)	
		)	BOARD OF
PATENT		)	
	MICHAEL R. FLEMING	)	APPEALS AND
	Administrative Patent Judge	)	
INTERFERENCES		)	
		)	
		)	
	ERIC FRAHM	)	
	Administrative Patent Judge	)	

MRF:psb

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