

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte UPENDRA M. KULKARNI

Appeal No. 96-0862
Application 08/055,971¹

ON BRIEF

Before KRASS, TORCZON and CARMICHAEL, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 6, 8 through 13, 15 through 19 and 21 through 26, all of the claims pending in the application.

¹ Application for patent filed April 30, 1993.

The invention is directed to a micro-code sequencer. More specifically, the present invention provides for a micro-code sequencer in which fewer clock cycles are wasted upon execution of branch conditions by employing two ports for outputting both a branch-taken and a branch-not-taken micro-code vector in parallel so that the logic unit processing the micro-code vectors has immediate access to the appropriate micro-code vector regardless of whether the branch is taken or not.

Representative independent claim 1 is reproduced as follows:

1. A device for processing micro-code, comprising:

micro-code means for providing sequences of micro-code vectors, said sequences of micro-code vectors including branch condition micro-code vectors, branch-taken micro-code vectors and corresponding branch-not-taken micro-code vectors, with each branch-taken micro-code vector and corresponding branch-not-taken micro-code vector sharing a common micro-address;

output means for outputting micro-code vectors from said micro-code means, with a branch-taken micro-code vector and a corresponding branch-not-taken micro-code vector being output substantially in parallel;

micro-code vector selection means, connected to said output means, for selecting between said branch-taken micro-code vector and said corresponding branch-not-taken micro-code vector;

micro-code vector address selection means connected to said micro-code means for selecting micro-code vectors to be output from said output means without retrieving stored addresses in said branch condition micro-vectors, said micro-code vector address selection means comprising a pointer for identifying said micro-vectors to be output and a plus one adder for incrementing addresses stored in said pointer on each clock cycle such that micro-code vector address selection means selects next sequentially stored micro-code vectors in said micro-code means after selecting branch condition micro-vectors; and

data path logic unit coupled to said output means for executing said micro-code vectors, wherein said data path logic unit executes said branch condition vectors a clock cycle after which said branch condition micro-code vectors are retrieved from said micro-code means.

The examiner relies on the following references:

Joyce et al. (Joyce)	4,087,857	May 2, 1978
Keller et al. (Keller)	5,377,335	Dec. 27, 1994

Claims 1 through 6, 8 through 10, 12, 13, 15 through 17, 19 and 21 through 26 stand rejected under 35 U.S.C. 103 as unpatentable over Keller. Claims 11 and 18 stand rejected under 35 U.S.C. 103 as unpatentable over Keller in view of Joyce.²

² It appears that the rejections of the claims under 35 U.S.C. 103 over Feil, U.S. Patent No. 5,058,007, and under 35 U.S.C. 102, as anticipated by Keller, have been withdrawn by the examiner as they are not repeated in the latest answer. Accordingly, these rejections are not before us on appeal.

Appeal No. 96-0862
Application 08/055,971

Reference is made to the briefs and answers for the respective positions of appellant and the examiner.

OPINION

We reverse.

The initial burden is on the examiner to establish a prima facie case of obviousness when applying a rejection under 35 U.S.C. 103. It is our view that the examiner has not done so in the instant case.

In the statement of the rejection and rationale therefor, at pages 2-4 of the supplemental answer (Paper No. 15), the examiner indicates various elements disclosed by Keller such as "a control store...", " a plurality of output ports...", "a plurality of latches..." and "a multiplexer..." However, the examiner never clearly indicates the correspondence, if any, between these elements and the instant claimed elements. Thus, it is not at all clear how the examiner is specifically applying the teachings of Keller.

Additionally, the examiner indicates that while Keller does not teach the storing of microinstructions in the control store in a sequential order in which the next microaddress is

Appeal No. 96-0862
Application 08/055,971

generated by incrementing the current microaddress by one, such storage in sequential order "is well known" [supplemental answer, page 3]. The examiner then concludes that it would have been obvious to apply "the implicit next address in Keller's control store to generate next non-branch microaddress by incrementing the current microaddress by one" [supplemental answer, page 4]. While the examiner alleges that a certain storage technique is "well known," the examiner has provided no such evidence. Moreover, it is unclear what claim limitation is alleged to be "well known."

The claims deal with micro-code vector selection means, micro-code vectors and micro-code vector address selection means wherein the latter comprises "a pointer for identifying said micro-vectors to be output and a plus one adder for incrementing addresses stored in said pointer on each clock cycle" so that the selection of the next sequentially stored micro-code vectors is performed "after selecting branch condition micro-vectors." The examiner has not pointed out how such limitations are seen to be disclosed or suggested by Keller.

Appeal No. 96-0862
Application 08/055,971

Furthermore, each independent claim specifically recites that the micro-code vectors to be output from the output means are selected "without retrieving stored addresses in said branch condition micro-vectors" [claim 12 omits "branch"]. This limitation permits the wasting of fewer clock cycles over the prior art. Yet, the examiner never satisfactorily explains how Keller suggests this limitation.

While appellant points out many differences between the instant claimed invention and the prior art mentioned in the specification, as well as Keller, [see, for example, the supplemental reply brief, pages 2-5], concluding, at page 5, that

[n]either Keller nor the prior art described in the specification teach [sic, teaches] or suggest [sic, suggests] a micro-code vector address selection means comprising a pointer for identifying a micro-vector to be output and a plus one adder for incrementing an address stored in the point [sic, pointer] on each clock cycle such that the micro-code vector address selection means selects a next sequentially stored micro-code vector from the micro code means after selecting branch condition vectors,

the examiner's response is merely to contend that the incrementing by one is "well-known in the art" [second supplemental answer, page 3] and that the selection of a

Appeal No. 96-0862
Application 08/055,971

particular addressing technique for addressing instructions "is generally an obvious engineering design choice" [second supplemental answer, page 3].

With regard to the claimed data path logic unit, the examiner contends [second supplemental answer, page 4] that the ability to fetch and execute sequential instructions in every clock cycle "is well-known and widely used in the prior art's processor."

Thus, the examiner makes many allegations regarding what is "well known" but provides no evidence of such. Further, there is no clear explanation as to how such "well known" elements and techniques are being applied to the specific claim language before us.

Accordingly, in our view, the examiner has failed to present a prima facie case of obviousness regarding the instant claimed subject matter and we will not sustain the rejection of claims 1 through 6, 8 through 13, 15 through 19 and 21 through 26 under 35 U.S.C. 103.

The examiner's decision is reversed.

Appeal No. 96-0862
Application 08/055,971

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
)	
)	
RICHARD TORCZON)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
JAMES T. CARMICHAEL)	
Administrative Patent Judge)	

Appeal No. 96-0862
Application 08/055,971

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