

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

\_\_\_\_\_  
Ex parte YOSHIYUKI ISHIMARU

\_\_\_\_\_  
Appeal No. 96-0439  
Application 07/956,497<sup>1</sup>

\_\_\_\_\_  
ON BRIEF

\_\_\_\_\_  
Before HAIRSTON, FLEMING and CARMICHAEL, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

***DECISION ON APPEAL***

This is a decision on appeal from the final rejection of claims 1 through 3, all of the claims pending in the present application.

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<sup>1</sup> Application for patent filed January 6, 1993.

The invention relates to a semiconductor device for controlling and driving display devices.

The independent claim 1 is reproduced as follows:

1. A semiconductor device comprising:

a semiconductor chip including segment signal outputting means having a plurality of output nodes for outputting segment signals for a display device controlled and selected by segment signals and scanning signals, and scanning signal outputting means having a plurality of output nodes for outputting scanning signals for the display device;

a first outlet-terminal group including a plurality of segment-signal outlet terminals arranged continuously at first and second, opposite sides of the semiconductor chip at predetermined intervals and respectively electrically connected to corresponding output nodes of the segment signal outputting means;

a second outlet-terminal group including a plurality of scanning-signal outlet terminals disposed along the first side of the semiconductor chip and arranged adjacent to the segment-signal outlet terminals at the first side of the semiconductor chip at predetermined intervals and respectively electrically connected to corresponding output nodes of the scanning signal outputting means; and

a third outlet-terminal group including a plurality of scanning-signal outlet terminals disposed along the second side of the semiconductor chip and arranged adjacent to the segment-signal outlet terminals at the second side of the semiconductor chip at predetermined intervals and respectively electrically connected to corresponding output nodes of the scanning signal outputting means.

The Examiner relies on the following references:

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Nakatani et al. (Nakatani) 1985 (UK Patent Application)	2,145,561	Mar. 27,
Ozaki 1990 (Japanese Patent Application)	2-131281	May 21,

Claims 1 and 2 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellant's admitted prior art shown in Figures 9 and 10 and Nakatani. Claim 3 stands rejected under 35 U.S.C.

§ 103 as being unpatentable over Appellant's admitted prior art shown in Figures 9 and 10 and Nakatani in further in view of Ozaki.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the briefs<sup>2</sup> and answer for the respective details thereof.

#### OPINION

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<sup>2</sup> Appellant filed an appeal brief on February 7, 1995. We will refer to this appeal brief as simply the brief. Appellant filed a reply appeal brief on July 7, 1995. We will refer to this reply appeal brief as the reply brief. The Examiner stated in the Examiner's letter dated October 19, 1995 that the reply brief has been entered. The Examiner provides no further response.

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We will not sustain the rejection of claims 1 through 3 under 35 U.S.C. § 103.

The Examiner has failed to set forth a *prima facie* case of obviousness. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983).

"Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), *citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

In regard to the rejection of claims 1 through 2 under 35 U.S.C. § 103 as being unpatentable over Appellant's admitted prior art shown in Figures 9 and 10 and Nakatani, Appellant argues on pages 5 through 10 of the brief that Appellant's

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admitted prior art shown in Figures 9 and 10 and Nakatani, together or individually, fail to teach or suggest "a third outlet-terminal group including a plurality of scanning-signal outlet terminals disposed along the second side of the semiconductor chip and arranged to the segment-signal outlet terminals at the second side of the semiconductor chip at predetermined intervals and respectively electrically connected to corresponding output nodes of the scanning signal outputting means" as recited in Appellant's claim 1. In particular, Appellant argues that all that Nakatani suggests as a modification of the prior art semiconductor shown in Figures 9 and 10 is the use of multiple semiconductor devices with leads bent in various different directions or the replacement of the printed circuit board including crossovers with an even more complex printed circuit board such as that illustrated in Nakatani's Figure 4. Appellant argues that Nakatani simply contains no discussion or suggestion that would have led those skilled in the art to modify the prior art Figures 9 and 10 to obtain the Appellant's invention.

The Examiner argues on page 3 of the answer that Nakatani teaches "a third outlet-terminal group" as recited in

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Appellant's claim 1. The Examiner states on page 3 of the answer that Nakatani teaches "the scanning electrodes may be divided into two groups (see page 3, lines 5-6) and that the LSI (64) may have output leads on opposing sides (see Figures 9 and 10) so that there are no wire crossings between the LSI and the flat matrix display panel (see page 3, lines 22-26), similar to applicant, relating to the third outlet-terminal group as claimed."

Appellant argues in the reply brief that reliance on Nakatani's LSI 64 for a teaching or even a suggestion of Appellant's claimed third outlet-terminal group is misplaced. Appellant points out that Nakatani teaches that the LSIs are mounted on a tape carrier so that the thus-package LSIs can be mounted in pairs with one LSI mounted face-up and the second of the LSI mounted face-down on a circuit substrate. The face-up/face-down pair arrangement avoids cross-over because of the pairs being mounted in a mutually inverted arrangement. Appellant argues that Nakatani does not teach or suggest a third outlet-terminal group as claimed.

Upon a closer inspection of Nakatani, we note that Nakatani states on page 2, line 129, through page 3, line 4,

"Y-electrodes (data electrodes) and a plurality of X-electrodes (scanning electrodes) are formed in a matrix fashion in a flat matrix display panel." Nakatani further teaches on page 3, lines 5-6, that either the X-electrodes or the Y-electrodes are divided into two groups. Nakatani teaches that in the preferred embodiment, the Y-electrodes 12 are divided into two groups ( $A_1$  through  $A_n$  and  $B_1$  through  $B_n$ ) as in the case of the system shown in Figure 1. Thus, Nakatani does not teach or suggest that both the data electrodes and the scan electrodes are divided into two groups.

Nakatani teaches on page 3, lines 14-44, an arrangement which solves the problem of avoiding crossing of the wiring between the LSIs. However, Nakatani does not solve the problem by providing a third outlet-terminal group as claimed by Appellant but by mounting on a circuit substrate one LSI face up and another LSI face down. Therefore, we find that Nakatani fails to teach or suggest Appellant's claimed invention.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the

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prior art suggested the desirability of the modification." **In re Fritch**, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), **citing In re Gordon**, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." **Para-Ordnance Mfg. v. SGS Importers Int'l**, 73 F.3d at 1087, 37 USPQ2d at 1239, **citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.**, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13. Upon reviewing Appellant's admitted prior art shown in Figures 9 and 10 and Nakatani, we fail to find any suggested desirability of modifying Appellant's admitted prior art shown in Figures 9 and 10 to provide a third outlet-terminal group to obtain Appellant's invention as recited in claims 1 and 2.

In regard to the rejection of claim 3 under 35 U.S.C. § 103 as being unpatentable over Appellant's admitted prior art shown in Figures 9 and 10 and Nakatani in further in view of Ozaki, we note that the Examiner relies on Nakatani for the teaching of a third outlet-terminal group. Thereby, we will not sustain this rejection for the same reasoning as above.

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We have not sustained the rejection of claims 1 through 3 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

**REVERSED**

	KENNETH W. HAIRSTON	)	
	Administrative Patent Judge	)	
		)	
		)	
		)	
	MICHAEL R. FLEMING	)	BOARD OF
PATENT	Administrative Patent Judge	)	APPEALS
		)	AND
		)	
INTERFERENCES		)	
	JAMES T. CARMICHAEL	)	
	Administrative Patent Judge	)	

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