

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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***Ex parte*** JAMES M. DOLAN, FRANK D. RAMIREZ  
and ROBERT J. TOLMIE JR.

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Appeal No. 95-5121  
Application 08/018,575<sup>1</sup>

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ON BRIEF

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Before THOMAS, HAIRSTON and CARMICHAEL, ***Administrative Patent Judges***.

CARMICHAEL, ***Administrative Patent Judge***.

***DECISION ON APPEAL***

This is an appeal from the final rejection of claims 1, 4-8, and 11-14, which constitute all the claims remaining in the application.

Claim 1 reads as follows:

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<sup>1</sup> Application for patent filed February 17, 1993.

1. Apparatus for commutation of a brushless motor having encoder means comprising a plurality of Hall-effect sensors operative for providing commutation information to a motor controller, the apparatus comprising an output drive section which includes three high-side power P-channel FETs and three low-side power N-channel FETs connected to determined stator windings of the brushless motor; a low-side pre-drive circuit operative to selectively turn on each of the low-side FETs and a high-side pre-drive circuit operative to selectively turn on each of the high-side FETs; a commutation decode logic circuit; an oscillator connected to the commutation decode logic circuit for providing a clock signal thereto; and, said commutation decode logic circuit being connected to the Hall-effect sensors to receive the commutation position information from the Hall-effect sensors and being connected to the high-side and low-side pre-drive circuits for providing selection signals for selecting the appropriate power FETs for commutating the motor, the apparatus also including an overcurrent detection and current limiting circuit connected to the low-side power FETs to monitor current through the motor.

The Examiner's Answer cites the following prior art:

Melocik et al. (Melocik)	4,514,665	Apr. 30, 1985
Reinhardt et al. (Reinhardt)	4,724,347	Feb. 9, 1988
Volz et al. (Volz)	4,843,288	Jun. 27, 1989
Gerschner et al. (Gerschner)	4,982,143	Jan. 1, 1991
Yaguchi	5,051,672	Sep. 24, 1991
Sei et al. (Sei)	5,216,293	Jun. 1, 1993
Le	5,258,696	Nov. 2, 1993

**OPINION**

Claims 1, 4, 5, 7, 8, 11, 12 and 14 stand rejected under 35 U.S.C. § 103 as unpatentable over Le in view of Volz, Reinhardt, Sei, Melocik, and Yaguchi. Claims 6 and 13 stand rejected under 35 U.S.C. § 103 as unpatentable over Le in view of Volz, Reinhardt, Sei, Melocik, Yaguchi and Gerschner.

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According to the examiner, it would have been obvious to reverse Le's p-n order as taught by Sei because this requires a large voltage difference to turn each transistor on and this in turn makes the system largely noise tolerant. Examiner's Answer at 3. Appellants argue that Sei did not suggest such a modification because Sei operates on CMOS components whereas Le employs power FETs.

The mere fact that the prior art may be modified in the manner suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. *In re Fritch*, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992).

In the present case, we find that Sei did not suggest the desirability of modifying Le as proposed by the examiner. Sei employs logic FETs, using logic level signals in a logic device. The p-n order may or not be reversed depending on the needs of the logic device. Column 5, lines 23-49. This is insufficient to suggest reversing the p-n order of Le's power FETs.

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**CONCLUSION**

The rejections are not sustained.

**REVERSED**

JAMES D. THOMAS	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
KENNETH W. HAIRSTON	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
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	)	
JAMES T. CARMICHAEL	)	
Administrative Patent Judge	)	

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