

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 50

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MASAKI TSUKUDE,
KAZUTAMI ARIMOTO
KAZUYASU FUJISHIMA,
YOSHIO MATSUDA
and TSUKASA OOISHI

Appeal No. 95-5032
Application 08/189,276¹

ON BRIEF

Before HAIRSTON, JERRY SMITH and FLEMING, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection

¹ Application for patent filed January 31, 1994. According to appellants, this application is a continuation of Application 07/938,582, filed September 2, 1992, now abandoned; which is a continuation of Application 07/735,684, filed July 29, 1991, now abandoned; which is a continuation of Application 07/441,588, filed November 27, 1989, now abandoned.

of claims 1-22, which constitute all the claims in the application.

The disclosed invention pertains to the area of a semiconductor memory apparatus. Such an apparatus includes a plurality of memory cells, sense amplifiers, word lines and bit line pairs. The invention has a hierarchical data organization in which corresponding bit line pairs are connected to respective memory cells over a pair of sub-I/O lines. A particular feature of the invention is in the manner in which control signals are applied to each sense amplifier in order to prevent erroneous coupling of transient voltages from one bit line to another.

Representative claim 1 is reproduced as follows:

1. In a memory apparatus including a plurality of memory cells, word lines and bit line pairs, said apparatus having a hierarchical data organization in which said plurality of memory cells are arranged in rows and columns, and a plurality of sense amplifiers and corresponding bit line pairs connected to respective memory cells receive data over a pair of sub-I/O lines corresponding to a plurality of said bit line pairs, wherein all the memory cells connected to a selected word line are selected and the pair of sub-I/O lines is connected to a corresponding bit line pair before activation of the plurality of sense amplifiers, a method of transferring data over said sub-I/O lines to said plurality of memory cells, comprising the steps of:

selecting a particular memory cell corresponding to a selected bit line pair;

receiving a plurality of distinct sense amplifier control signals, each sense amplifier control signal being distinct for each sense amplifier associated with a common pair of sub-I/O lines;

connecting one bit line pair of said plurality of bit line pairs corresponding to said selected memory cell to said sub-I/O lines; and

in response to the distinct sense amplifier control signals, activating the sense amplifier connected to said selected bit line pair; whereby

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coupling of transient voltage from said bit line corresponding to said particular memory cell to others of said bit lines through said sense amplifiers is prevented.

The examiner relies on the following references:

Itoh et al. (Itoh)	4,590,588	May 20, 1986
Taguchi et al. (Taguchi)	4,791,616	Dec. 13, 1988
Koyanagi	4,970,685	Nov. 13, 1990 (filed Jan. 18, 1989)

The admitted prior art of Figures 1-4 of the specification.

Claims 1-22 stand rejected under 35 U.S.C. § 103. As evidence of obviousness the examiner offers Taguchi in view of the admitted prior art with respect to claims 1-11, 13-16 and 18-22, and Taguchi in view of the admitted prior art and Koyanagi or Itoh with respect to claims 12 and 17.

Rather than repeat the arguments of appellants or the examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the collective evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1-3 and 9-17. We reach the opposite conclusion with respect to claims 4-8 and 18-22. Accordingly, we affirm-in-part.

Appellants have nominally indicated that the claims do not stand or fall together [brief, page 5], but they have not specifically argued the limitations of each of the claims. To the extent that appellants have properly argued the reasons for independent patentability of specific claims, we will consider such claims individually for patentability. To the extent that appellants have made no separate arguments with respect to some of the claims, such claims will stand or fall with the claims from which they depend. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

At the outset, before the scope of the claims and the teachings of the references are considered, an issue has been raised as to whether Figures 3 and 4 of the specification are available as prior art against these claims on appeal. The examiner's rejections, as noted above, rely on Figures 3 and 4 as admitted prior art. Appellants argue that these figures should not be considered as prior art in this case. The facts are not in dispute.

The specification begins by describing Figures 1-4 in the section entitled "BACKGROUND OF THE INVENTION." Figures 1 and 2 are labeled "prior art" and appellants admit that these figures are

prior art. Figure 3 is described as an improvement on the memory of Figure 1 since it reduces the parasitic capacitance of the bit line pairs due to the number of memory cells. The memory of Figure 3 achieves this reduction by dividing the single bit line pair into a plurality of bit line pairs and connecting each of the divided bit line pairs to a single sub-input/output line pair through transfer gates. The description of Figures 1-4 is followed by a section entitled "SUMMARY OF THE INVENTION." The summary of the invention states its object as "to solve the above described problems" (presumably meaning the problems caused by the circuits shown in Figures 1 and 3). This section is followed by a section entitled "BRIEF DESCRIPTION OF THE DRAWINGS." The original specification describes Figures 1 and 3 as follows:

Fig. 1 is a circuit diagram showing a structure of a conventional two-port memory device;

Fig. 3 is a circuit diagram showing one example of a semiconductor memory device which is not prior art but is considered to be the background of the present invention; [specification, page 11].

The examiner has been relying on Figure 3 as prior art since a rejection was made in the grandparent application to this application [S. N. 07/735,684]. The examiner has consistently maintained his position since that time that Figures 1-4 were all considered to be admitted prior art. Appellants began referring to Figures 3 and 4 as "prior art" after the examiner designated them as such. Appellants referred to Figure 3 as prior art in papers filed July 29, 1992, June 24,

1993, January 31, 1994 and September 13, 1994. It was not until after the final rejection was made in this application on November 16, 1994 that appellants first argued that Figures 3 and 4 were not prior art.

It is the position of the examiner that since the record in this case is inconsistent, and since appellants have admitted more than once that Figures 3 and 4 are prior art, that appellants' repeated admissions of prior art now make it so [answer, pages 6-7]. Appellants argue that any previous reference to Figures 3 and 4 as prior art and the reference to Figure 3 as being "conventional" were unintentional errors. Appellants assert that these unintentional errors do not "act as an 'uncorrectable' admission that the figure is prior art when the error is discovered" [brief, pages 11-13]. Based on the facts of record here, we agree with the examiner that Figures 3 and 4 are available as prior art with respect to the claimed invention for reasons which follow.

We agree with appellants that the alleged inadvertent error made here can be corrected. Nevertheless, we are of the view that the erroneous admission cannot be corrected simply by stating that it was erroneous. Although an admission by itself can create a presumption that something is prior art, the admission cannot be overcome by simply repudiating the admission. In other words, the factual showings to support an admission of prior art are very different from the showings necessary to overcome such a presumption. Appellants' reference to Figures 3 and 4 as prior art was sufficient to legally support a presumption that the figures were prior art with respect to appellants, and this

presumption has not been overcome by appellants' bare denial.

Part of the problem is that it is not clear what is meant by appellants' statement now that Figures 3 and 4 are not prior art. Appellants could mean that Figures 3 and 4 are not prior art under any section of 35 U.S.C. § 102 which assertion would not be sufficient to prove that they are not prior art against appellants in this case. It has been held that certain prior art may be prior art to one inventive entity, but not to the public in general. See, for example, In re Fout, 675 F.2d 297, 300-301, 213 USPQ 532, 535 (CCPA 1982). Thus, in order to make the legal determination that Figures 3 and 4 are not prior art with respect to appellants, one needs to know exactly where these figures came from and how appellants became aware of these figures. Appellants are in a unique position to explain how they became aware of the circuit of Figure 3 and as to whether the circuit of Figure 3 is prior art with respect to them.

Fout also stands for the proposition that an appellants' invention should be judged on obviousness against their actual contribution to the art. Thus, if Figures 3 and 4 do not represent the work of appellants, then it would be proper to conclude that these figures form no part of appellants' invention and are prior art with respect to appellants. It is noteworthy that the device of Figure 3 has the kind of problems which appellants' invention is designed to correct [SUMMARY OF THE INVENTION, supra]. This discussion of the invention in appellants' specification also raises the presumption that Figure 3 is not the invention, but rather, the invention was designed to correct the problems created by

the known or conventional circuit of Figure 3. It would not normally be expected that the circuit of Figure 3 be invented with a specific problem so that an invention could be designed to solve the problem. The natural assumption would be that the circuit of Figure 3 was known to those persons skilled in this art, and appellants' invention was directed to solving a known problem with this circuit.

In summary, the facts in this case raise a rebuttable presumption that Figures 3 and 4 are prior art with respect to appellants, and appellants have not provided the kind of evidence necessary to overcome this presumption. Therefore, we agree with the examiner that Figures 3 and 4 of this application may be used as prior art against appellants with respect to these claims. We now consider the arguments of appellants and the examiner which are directed to the merits of the rejection. Appellants' first argument is that the sense amplifiers in their invention are controlled in a manner which is different from the control of Taguchi. Specifically, appellants argue that "each sense amplifier control signal being distinct for each sense amplifier associated with a common pair of sub-I/O lines" must be read as each pair of signals SAE1 and the inverse of SAE1 and SAE2 and the inverse of SAE2 as disclosed [brief, page 15]. The examiner responds that the quoted language does not require that the control signals have an inverted relationship or occur at the same time [answer, pages 7-8]. In other words, the examiner asserts that appellants' arguments are not commensurate in scope with the claimed invention.

Taguchi shows two sense amplifiers in his Figure 6. One sense amplifier receives the signals N_s

and N_{LE} while the other sense amplifier receives the signals N_S and N_{LE} . Thus, four distinct and recognizable control signals are used in the Taguchi memory device. The claims recite that each of the sense amplifier control signals is distinct for each sense amplifier. We agree with the examiner that the four control signals of Taguchi meet this claim language since each of the control signals is distinct from the others. Appellants' interpretation of the claim language is stricter than the language requires.

Appellants argue next that the independent claims require that the pair of sub-I/O lines be connected to a selected bit line pair "before activation of the plurality of sense amplifiers" [brief, page 16]. According to appellants, neither Taguchi nor Koyanagi nor Itoh suggests this relationship. The examiner responds that this limitation is met by the admitted prior art of Figure 3. Appellants again argue that Figure 3 of this application is not prior art. Since we determined above that Figure 3 is available as prior art, this particular argument of appellants is not persuasive.

Claims 12 and 17 were separately rejected using the additional teachings of Koyanagi or Itoh. Appellants argue that these claims "are patentable over the applied references for reasons similar to those for claims 1-3, 9-11 and 13-16" [brief, pages 17-18]. Since we have previously determined that appellants' arguments with respect to these claims are not persuasive of error by the examiner, we find no error in the rejection of claims 12 and 17.

Appellants separately argue claims 4-8 and 18-22 as reciting means for generating the timing signal which "means" has not been appropriately considered by the examiner under the last paragraph

of 35 U.S.C. § 112. According to appellants, the timing signal generating circuitry of the invention is depicted in Figure 8 of the application, and the recitations of these claims must be construed to cover the circuitry of this figure and its corresponding description in the specification [brief, pages 18-19]. Appellants correctly point out that neither Taguchi nor Figure 3 of this application shows any circuitry for generating clock signals. Appellants conclude that there can be no basis for concluding that Taguchi discloses the same or equivalent circuitry when there is no circuitry disclosed at all for performing the recited functions. The examiner has either overlooked or ignored this argument by appellants because the answer is silent on this issue.

There is no evidence in this case that the claim interpretations mandated by the last paragraph of 35 U.S.C. § 112 have ever been considered by the examiner. On this record, it appears to us that the following two questions must still be answered: (1) what structure should be read into the claims corresponding to the timing signal generating means? and (2) does the applied prior art suggest the obviousness of this structure?

Appellants have answered the first question by asserting that the structure of Figure 8 of the application must be read into the claims in interpreting claims 4-8 and 18-22. Appellants have presented a reasonable argument as to why the timing signal generating means of these claims cannot be supplied by the missing disclosure in each of the applied prior art references. The examiner has failed to respond as to how the applied prior art can be interpreted to meet the invention of claims 4-8 and

18-22 when they are given the interpretation mandated by the last paragraph of 35 U.S.C. § 112. As noted above, the examiner has not addressed this question at all. For reasons we have discussed above, the issue of claim interpretation under 35 U.S.C. § 112 has been properly raised by appellants but has not been considered by the examiner on this record. The examiner is required to make factual showings in response to properly raised questions as to how the applied prior art teaches the structure of claimed means or an equivalent thereof. The examiner has made no such factual showings in this case.

Thus, appellants' arguments regarding the proper interpretation of the claims stand essentially unrebutted by the examiner, and we find these unrebutted arguments to be logical, accurate and persuasive. Therefore, the invention of claims 4-8 and 18-22 should be construed in the manner argued by appellants. Such claim construction has not been considered by the examiner on this record. Accordingly, we conclude that the examiner has failed to support his position that the claimed timing signal generating means would have been obvious to the artisan in view of the applied prior art. Therefore, we do not sustain the rejection of claims 4-8 and 18-22 as formulated by the examiner.

No other claims are separately argued by appellants. Therefore, in view of our discussion above, we sustain the rejection of claims 1-3 and 9-17 but we do not sustain the rejection of claims 4-8 and 18-22. Accordingly, the decision of the examiner rejecting claims 1-22 under 35 U.S.C. § 103 is affirmed-in-part

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON
Administrative Patent Judge

JERRY SMITH
Administrative Patent Judge

MICHAEL R. FLEMING
Administrative Patent Judge

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