

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALEXANDER J. LIMBERIS
JOANNE F. OTTNEY and
JOSEPH W. BRYAN

Appeal No. 95-4736
Application 08/084,801¹

ON BRIEF

Before URYNOWICZ, HAIRSTON and BARRETT, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claims 1-39, all the claims pending in the application.

The invention pertains to apparatus for replacing segments of instructions for a processor.

Claims 1 and 14 are illustrative and read as follows:

¹ Application for patent filed June 29, 1993.

1. An apparatus for replacing a segment of instructions for a processor, the processor responsive to instructions to change data, comprising:

a memory system coupled to the processor having a set of memory locations to supply a sequence of instructions stored in the set of memory locations to the processor;

a controller, coupled to the memory system and the processor, and having an input, that is responsive to a command on the input to disable the processor from changing data in response to instructions from a particular subset of the set of memory locations which stores the segment of instructions, the particular subset including more than one memory location; and

a memory interface, coupled to the memory system and to the controller, to receive and write new instructions to the particular subset to replace the segment of instructions.

14. A signal processing system comprising:

a real time processor to execute a plurality of segments of instructions;

an instruction memory coupled to the real time processor having a plurality of memory locations with respective addresses, to store the plurality of segments of instructions in respective groups of addresses and output a sequence of instructions to the real time processor in response to addresses;

a sequencer coupled to the instruction memory operative to provide a sequence of addresses identifying the sequence of instructions in the instruction memory;

a controller, coupled to real time processor, the instruction memory and the sequencer, operative, in response to a command, to override execution of a particular segment of instructions stored in a particular group of addresses in the instruction memory, the particular segment including more than one instruction; and

a host interface coupled to the instruction memory and the controller for receiving and writing new instructions to the instruction memory in the particular group of addresses to replace the particular segment of instructions.

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The references relied upon by the examiner as evidence of obviousness are:

Dube et al. (Dube)	4,654,817	Mar. 31, 1987
Littleton	5,109,504	Apr. 28, 1992

The appealed claims stand rejected under 35 U.S.C. § 103 as obvious over Littleton in view of Dube.

The respective positions of the examiner and the appellants with regard to the propriety of this rejection are set forth in the final rejection (Paper No. 6) and the examiner's answer (Paper No. 14) and the appellants' brief (Paper No. 13).

Appellants' Invention

Appellants' invention relates to audio processors such as music synthesizers, real time processors in other fields and, in general, any computer system which executes a set of programs and has a need to replace programs in the set during run time. In Figure 2, which shows a microprocessor designed for use with a music synthesizer, a set of programs is stored in a microcode store 213. Instructions are supplied through pre-fetch device 214 to a decoder 550 which controls execution of the instructions by the processor. When one program in the set of programs stored in the microcode store 213 needs to be replaced, a command is supplied through

a host interface 200 into the NOP controller 500 to initiate the process. The NOP controller 500 signals the decoder 550 with a NOP flag across line 503. In response to the flag, write enable signals on line 553 which are generated by the decoder 550 are turned off. Thus, when an instruction is decoded from the set of locations to be overridden, it will have no effect on any stored data in the processor. The processor is disabled from changing data in response to instructions in the particular set of memory locations in the microcode store 213 which stores the program being replaced. While the NOP flag is produced, the pre-fetch mechanism 214 continues to sequence through the instructions in the microcode store 213, and the set of instructions for the new program is loaded into the microcode store at the appropriate location through the host interface 200. Thus, the programs stored in the microcode store 213 which are not being replaced continue to execute properly, without interruption, while the program being replaced is disabled and a new program is substituted. After the operation is complete, the NOP controller 500 stops asserting the NOP flag 503 so the new program is executed next time the pre-fetch mechanism sequences through the set of locations.

Opinion

Appellants contend that the rejection of claims 1-39 is insufficient because the combination of references does not describe specific limitations in the rejected claims, and the combination taken as a whole does not otherwise suggest such limitations in the claimed subject matter. With respect to independent claim 1, it is alleged that neither reference teaches disabling a processor from changing data in response to instructions from a particular subset of instructions which are

to be replaced. With respect to independent claims 14 and 28, appellants contend that neither reference involves replacing, during system run time, stored instructions with new instructions in the particular group of addresses the stored instructions are located in.

After consideration of the positions and arguments presented by both the examiner and the appellants, we have concluded that the rejection of claims 1-39 should not be sustained.

With respect to claim 1, both the examiner and appellants agree that neither reference teaches a controller which performs the disabling function of the claim, and we are of the opinion that it has not been established that this prior art taken as a whole would have suggested to one of ordinary skill in the art to modify the teachings of the art to include the disabling function. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-1784 (Fed. Cir. 1992). The examiner's position that it would have been obvious to one of ordinary skill in the art to recognize that control means must disable read/write results of execution during the process of interruption is not persuasive. The examiner seems to be saying that it would have been obvious to disable Littleton's system during data substitution. Even assuming that this is true, this is not what appellants are doing. The disablement disclosed and claimed by appellants is not a general disablement of the entire system; rather, it is a specific type of disablement. At page 9 of appellants' specification, it is disclosed that the NOP controller causes instructions stored in the

portion of the MSP memory allocated for replacement to be disabled from changing the contents of memory locations in the processor or managed by the processor. The other voice programs in the MSP memory are not affected by the NOP controller, and the MSP module continues to execute those voice programs. Claim 1 requires a controller to disable the processor from changing data in response to instructions from a particular subset of the set of memory locations which stores the segment of locations to be replaced.

With respect to claims 14 and 28, we agree with appellants that neither reference teaches replacing stored instructions with new instructions in the particular group of addresses the stored instructions are located in. Littleton teaches replacing a stored or obsolete instruction with an interrupt trap. The new instruction, however, is located at a different address indicated by a trap number. Column 5, lines 42-48. The new instruction is not disclosed as stored in the particular address the stored instruction is located in. Otherwise, it has not been established that the claimed subject matter would have been an obvious modification of Littleton and Dube. The examiner has set forth no reason or suggestion why one of ordinary skill in the art would have made such a modification.

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In view of our opinion with respect to the rejection of independent claims 1, 14 and 28 over Littleton and Dube, the rejection of dependent claims 2-13, 15-27 and 29-39 over this prior art will not be sustained.

REVERSED

STANLEY M. URYNOWICZ)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
KENNETH W. HAIRSTON)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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