

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KAZUMI KURIMOTO,
AKIRA HIROKI, and SHINJI ODANAKA

Appeal No. 95-4641
Application 08/023,122¹

HEARD: Oct. 14, 1997

Before KRASS, SMITH, JERRY, and CARMICHAEL, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 3 and 5 through 14, constituting all the claims remaining in the application.

The invention is directed to a MIS transistor having a gate sidewall insulating layer. The structure of the instant invention is

¹ Application for patent filed February 26, 1993. According to appellant, this application is a division of Application 07/780,760, filed October 25, 1991, now U.S. Patent No. 5,221,632.

said to avoid occurrence of hot-electron deterioration due to moderation of the horizontal electrical field of the low density (source-drain) diffusion layer provided by a first gate side wall having a high dielectric constant. Further, with the provision of a second gate side wall insulating film which covers all of the surfaces of the first gate side wall that are not in contact with an insulating film, it is said that the capacitance between the gate electrode and the wiring above the gate can be reduced.

Independent claim 1 is reproduced as follows:

1. A MIS transistor, comprising:

a semiconductor substrate of a first conduction type;

a gate insulation film and a gate electrode which are selectively formed on said semiconductor substrate;

a second insulating film having a first portion formed on a side surface of said gate electrode and a second portion formed on said semiconductor substrate;

a first gate side wall film provided on a surface of said first portion of said second insulating film and a surface of said second portion of said second insulating film and having a dielectric constant greater than that of said second insulating film, said first gate side wall film having a height smaller than that of said gate electrode;

a low density diffusion layer of a second conduction type formed on said semiconductor substrate so as to be disposed below and around said gate electrode so that each end part of said gate electrode overlaps said low density diffusion layer; and

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We turn first to the rejection under 35 U.S.C. § 112, second paragraph. We will not sustain this rejection.

The examiner makes the following observations at page 4 of the answer:

In claim 1, line 8, and claim 3, lines 6-7, claims 7, 9, 11, [sic, and] 13, the phrase "first gate side wall" is unclear whether it is being referred to the first gate side wall insulating film.

In claim 1, lines 14-17, it is unclear how the low density diffusion layer of a second conduction type [sic, is?] formed on the semiconductor below and around the gate electrode.

In claim 3, lines 3-6, it is unclear how the high density diffusion layer [sic, is?] formed on the semiconductor substrate below and around the first gate side wall insulating film.

In claim 6, lines 2-4, it is unclear how a high density diffusion layer [sic, is?] formed on the semiconductor substrate and below and around the gate electrode.

Regarding the examiner's problem with the recitation of "first gate side wall," appellants amended this language to read "a first gate side wall film" in the amendment filed September 22, 1994 (Paper No. 9) in response to the final rejection; yet the examiner maintains the rejection without explanation as to why this amendment does not overcome the rejection.

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With regard to the rest of the rejections under 35 U.S.C. § 112, second paragraph, they all seem to be directed to the "below and around" language appearing in the claims. Appellants have explained that reference to the drawings clearly shows that the recited diffusion layers are formed "below and around" the cited structures, as claimed. For example, low density diffusion layer 8 is shown as being formed "below and around" the gate electrode 3; the high density diffusion layer 9 is shown formed "below and around" the first gate side wall insulating film 5 and "below and around" the gate electrode 3.

Accordingly, since the examiner's rejections under 35 U.S.C. § 112, second paragraph, appear unreasonable in view of appellants' amendments and in view of what is clearly shown in the drawings, we will not sustain the rejection of claims 1, 3 and 5 through 14 under 35 U.S.C. § 112, second paragraph.

We turn now to the rejection of claims 1, 3 and 5 through 14 under 35 U.S.C. § 103.

The examiner cites, in particular, Figure 2(d) of Tsukura as disclosing the transistor as claimed but for the disclosure of a lightly doped diffusion region formed below a sidewall of the gate electrode. The examiner then cites Chen for the teaching of a lightly doped n-type region formed below a gate electrode wherein the

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gate electrode has a sidewall which reaches a position above the n-type region in Figure 1(c). Finally, the examiner concludes [answer, page 6] that since both Tsukura and Chen

teach a high dielectric constant sidewall material formed adjacent to the gate electrode, it would have been obvious...to have the N-type region of Chen...in Tsukura because it prevents occurrence of hot-electron deterioration in MOS device.

We do not view the examiner's combination of Tsukura and Chen as being proper under 35 U.S.C. § 103. Tsukura teaches no overlap of the gate electrode 12 with the diffusion region 15. Chen does show such an overlap in Figure 1(c). What is then needed for a proper rejection under 35 U.S.C. § 103 is a reason for combining these disparate teachings. With references, throughout the translation of Tsukura, of forming the source-drain region "by self-alignment" and that the source and drain regions "do not intrude as far as the channel region portion directly under the gate electrode," it is clear that Tsukura intends to specifically prevent the claimed overlap. On the other hand, the overlap is essential in Chen in order to provide immunity to hot electrons. Therefore, we agree with appellants that the teachings of these references are "mutually exclusive" [principal brief, page 5] and that

Because the express object of the Tsukura invention is to overcome disadvantages in

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the type of device disclosed by the Chen et al reference. . . , the teachings of Tsukura and Chen et al cannot properly be combined [principal brief, page 6].

The examiner's reasoning for making the combination, at page 8 of the answer, regarding the desire to prevent the occurrence of hot-electron deterioration in the MOS device of Tsukura, appears to us to be based more on hindsight, with appellants' specification in view, than on any suggestion provided by the applied references.

Accordingly, we will not sustain the rejection of claims 1, 3 and 5 through 14 under 35 U.S.C. § 103.

The examiner's decision is reversed.

REVERSED

Errol A. Krass)	
Administrative Patent Judge)	
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Jerry Smith)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
James Carmichael)	
Administrative Patent Judge)	

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