

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KUNIHIRO TSUTSUMI

Appeal No. 95-4183
Application 07/945,714¹

HEARD: July 17, 1997

Before KRASS, BARRETT and TORCZON, Administrative Patent Judges.
KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claim 14, the sole claim remaining in the application.

¹ Application for patent filed September 15, 1992.

The invention pertains to a video image display device as described by claim 14 reproduced as follows:

14. A video image display device comprising:

an address selector circuit responsive to a line selection signal for determining a vertical position on a display screen and a column selection signal for determining a horizontal position on the display screen to produce a first address signal and a second address signal;

a display data random access memory for storing all character codes to be displayed and reading and outputting one of said character codes stored in an address indicated by said first address signal;

a single chip IC character generator comprising a read only pattern memory for storing a plurality of character patterns each composed of a plurality [sic, of] pattern lines each composed of a bit pattern, and an address determination circuit and a selector circuit operable, in response to said character code and said second address signal, to select one of said character patterns corresponding to said character code and output a bit pattern signal of one of said pattern lines corresponding to said second address signal; and

a serial converter circuit responsive to a fringe request signal from a microcomputer to generate a bit pattern of fringe for said bit pattern of said character pattern and output signals of said fringe bit pattern and said bit pattern of said character pattern dot by dot every clock having a period corresponding to a horizontal scan period of respective display dots on the display screen,

wherein said read only pattern memory stores all of said pattern lines of each of said character patterns, and selects, in response to said character code, one of said character patterns and outputs said bit pattern of said selected character pattern corresponding to said second address signal when a value of said second address signal indicates any of said pattern lines;

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OPINION

We will not sustain the rejection of claim 14 under 35 U.S.C. 103 in view of Kitano because the examiner has failed to establish a prima facie case of obviousness with regard to the claimed subject matter.

Claim 14 calls for, inter alia,

a serial converter circuit responsive to a fringe request signal from a microcomputer to generate a bit pattern of fringe for said bit pattern of said character pattern and output signals for said fringe bit pattern and said bit pattern of said character pattern dot by dot every clock having a period corresponding to a horizontal scan period of respective display dots on the display screen...

The examiner contends [page 2 of the second supplemental answer] that "the claimed fringe bit pattern or bit pattern of spaces reads on the generated spaces of Kitano..." While the examiner has previously explained why he regards the previously claimed bit pattern of spaces as being obvious over

patentability of claim 14 in view of Kitano is basically treated in the second supplemental answer (Paper No. 21, August 6, 1996) and the supplemental reply brief (Paper No. 22, October 7, 1996). The issue was narrowed down to the patentability of claim 14, solely, with the cancellation of claims 8 through 10, 12 and 13 by the amendment of March 7, 1995 (Paper No. 19).

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the disclosure of Kitano, it is unclear how anything taught by Kitano relates to the "bit pattern of fringe" recited in instant claim 14. Kitano indicates nowhere in the disclosure that a fringe or a bit pattern of fringe is of any interest.

A "fringe," according to the instant specification is a border around a character used where a character may be displayed on a background having the same color as the character. See, for example, page 18 of the instant specification:

...when a white colored character pattern is displayed on a white background it is difficult to distinguish the character pattern without fringe, the character pattern is emphasized if black-fringed and easily distinguished regardless of background state.

The fringe is generated, in accordance with page 17 of the instant specification, as follows:

...the character generator 7 receives the character code G and the address signal L and outputs bit pattern signals of the character pattern line "P" and character pattern lines above and below the line according to the address signal L when a fringe is requested.

The serial conversion circuit 8 which receives these three character pattern lines produces a fringe pattern "Y" and outputs bit pattern signals of the character pattern "P" and the fringe pattern "Y" serially dot by dot.

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We find nothing in Kitano related to such a fringe and it is unclear to us how or why the examiner equates a fringe bit pattern with a bit pattern of spaces and how or why such a fringe bit pattern "reads on the generated spaces of Kitano," as contended by the examiner. Looking at the instant claim language, since there is no fringe, as disclosed and claimed by appellant, in Kitano, it is difficult to perceive how Kitano can be said to disclose or suggest a serial converter circuit "responsive to a fringe request signal from a microcomputer to generate a bit pattern of fringe..."

We note, in passing, that the background section of the instant specification, at pages 2-4, appears to indicate that the generation of fringe patterns around characters in a video display device was known and even that the fringe pattern was generated as a bit pattern by a serial conversion circuit on the basis of adjacent dot values [see page 3 of the specification]. However, this disclosure forms no part of the basis for the examiner's rejection and we offer no opinion as to whether such disclosure could have been properly combinable with Kitano to suggest the instant claimed subject matter. We make the observation merely to indicate that there are prior art teachings of fringe generation and the examiner may wish to consider this

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but Kitano, alone, clearly does not suggest the claimed fringe request signal and generation of a bit pattern of fringe.

The examiner's decision rejecting claim 14 under 35 U.S.C. 103 over Kitano is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
)	
)	
LEE E. BARRETT)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
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RICHARD TORCZON)	
Administrative Patent Judge)	

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