

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 32

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHINICHI SATOH, HIROJI OZAKI and
TAKAHISA EIMORI

Appeal No. 95-2599
Application 07/983,931¹

ON BRIEF

Before HAIRSTON, FLEMING and TORCZON, **Administrative Patent
Judges.**

FLEMING, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on appeal from the final rejection of

¹Application for patent filed December 1, 1992. This application is a continuation of Application 07/787,912 now U.S. Patent 5,543,646 issued August 6, 1996, which is a continuation of Application 07/242,116, now U.S. Patent No. 5,089,863, issued February 18, 1992.

claims 6, 8 through 10, 22, 24 and 25. Claims 1 through 5, 7, 11 through 21 and 23 have been canceled.

The invention relates generally to a field effect transistor. Appellants disclose on pages 3 and 4 of the specification that N⁺ impurities are diffused in a transverse direction producing an overlapping portion in a distance)L under gate electrode 3 as shown in Figure 1C. This overlapping portion constitutes an additional capacitance between the gate and the source-drain preventing the transistor from operating at a high speed as well as increasing the power consumption of the transistor.

On page 9 of the specification, Appellants disclose that they solved this problem by forming a field effect transistor with a T-shaped gate electrode 3 having a lower layer 3a and an upper layer 3b as shown in Figure 4A. On page 12 of the specification, Appellants disclose that the lower layer 3a and the upper layer 3b are etched by a known plasma etching method as shown in Figure 5C. The lower layer 3a and the upper layer 3b are formed of the same base composition, i.e. polysilicon. However, Appellants disclose that these layers contain a differing chemical or physical feature which provides the lower layer 3a with a faster etch rate as compared with the upper layer

etch rate. Appellants disclose on pages 12 and 13 of the specification that one physical feature difference between the two layers which would allow for a different etch rate is grain size. Appellants disclose that the upper and lower layers may be formed of polysilicon wherein the grain size of the polysilicon in the upper layer is different from that of the lower layer. Appellants disclose on pages 13 and 14 of the specification that another difference that would provide the lower layer 3a with a faster etch rate than the upper layer 3b is ion impurity concentration. Appellants disclose that by providing the upper layer with a first ion impurity concentration and the lower layer with a second ion impurity concentration wherein the second ion impurity concentration is greater than the first ion impurity concentration, the lower layer 3a will have a faster etch rate than the upper layer 3b.

The independent claim 25 is reproduced as follows:

25. A field effect transistor comprising:

a semiconductor substrate having a main surface and a pre-determined impurity concentration of a first conductivity type;

impurity layers of a second conductivity type formed spaced apart at the main surface of the semiconductor substrate, said impurity layers constituting source-drain regions, each of the impurity layers comprising a first impurity layer portion having a first impurity concentration and a second impurity layer portion

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having a second impurity concentration which is higher than the first impurity concentration, the first impurity layer portions defining a first channel region at the main surface of the substrate and the second impurity layer portions defining a second channel region, the first impurity layer portions being shallower throughout the substrate as compared with the second impurity layer portions; and

a shaped conductive layer formed by etching on said first channel region with an insulating film interposed therebetween at said main surface, said shaped conductive layer having an upper portion and a lower portion, the upper portion having a flat upper surface and being longer than the lower portion, the length of the lower portion adjacent the insulating film being substantially equal to or shorter than the length of said first channel region, the width of the second channel region being no greater than the length of the upper portion upper surface, and the upper and lower portions being formed of the same material, with the lower portion having a faster etch rate as compared with an etch rate of the upper portion under the same etching conditions, and wherein there is only insulating film between outermost ends of the shaped conductive layer upper portion and the main surface of the substrate.

The Examiner relies on the following reference:

Sato et al. (Sato) 63-044770 Feb. 25, 1988
(Japanese Kokai)

Claims 6, 8 through 10, 22, 24 and 25 stand rejected under 35 U.S.C. § 102 as anticipated by Sato or in the alternative claims 6, 8 through 10, 22, 24 and 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sato. In the supplemental Examiner's answer, the Examiner sets forth a new ground of

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rejection wherein claims 6, 8 through 10, 22, 24 and 25 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims 23, 26, 33 and 34 present in copending application, serial no. 07/787,912².

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs³ and answers⁴ for the

²Now U.S. Patent No. 5,543,646 issued August 6, 1996. In view of the issuance of a patent, the rejection is no longer characterized as a provisional rejection.

³ Appellants filed an appeal brief on November 2, 1994. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on February 13, 1995. We will refer to this reply appeal brief as the reply brief. The Examiner stated in the supplemental Examiner's answer mailed April 26, 1995 that the reply brief has been entered and considered. Appellants filed a supplemental reply appeal brief on June 26, 1995. We will refer to this supplemental reply appeal brief as the supplemental reply brief. The Examiner stated in an Examiner's letter, mailed July 3, 1995, that the supplemental reply brief has been entered and considered.

⁴The Examiner responded to the brief with an Examiner's answer, mailed December 13, 1994. We will refer to the Examiner's answer as simply the answer. The Examiner responded to the reply brief with supplemental Examiner's answer, mailed April 26, 1995. We will refer to the Supplemental Examiner's answer as simply the supplemental answer. The Examiner responded to the supplemental reply brief with a letter, mailed July 3, 1995 stating that the supplemental reply brief had been entered and clarified that claims 6, 8 through 10, 22, 24 and 25 are provisionally rejected under the judicially created doctrine of

(continued...)

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respective details thereof.

OPINION

After careful consideration, we will sustain the Examiner's rejection of claims 6, 8 through 10, 22, 24 and 25.

At the outset, we note that Appellants have indicated on page 7 of the brief that claims 6, 8, 22 and 24 stand or fall together with claim 25 and that claims 9 and 10 are independently patentable over claim 25. 37 CFR § 1.192(c)(5) amended October 22, 1993 states:

For each ground of rejection which appellant contests and which applies to more than one claim, it will be presumed that the rejected claims stand or fall together unless a statement is included that the rejected claims do not stand or fall together, and in the appropriate part or parts of the argument under subparagraph (c)(6) of this section appellant presents reasons as to why appellant considers the rejected claims to be separately patentable.

As per 37 CFR § 1.192(c)(5), which was controlling at the time of Appellants' filing the brief, we will, thereby, consider Appellants' claims 6, 8, 22, 24 and 25 to stand or fall together,

⁴(...continued)
obviousness-type double patenting as being unpatentable over the claims 23, 26, 33 and 34 present in copending application, serial no. 07/787,912 (now U.S. Patent 5,543,646 issued August 6, 1996).

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with claim 25 being considered the representative claim and we will consider claims 9 and 10 separately.

Appellants argue on pages 9 and 10 of the brief that Sato fails to teach that when the substrate-side and the surface-side portions are formed of the same material the substrate-side portion has a faster etch rate as compared with an etch rate of the surface-side portion under the same etching conditions. The Examiner argues that the claimed limitations setting forth that the lower portion has a faster etch rate as compared with an etch rate of the upper portion under the same etching conditions as recited in Appellants' claim 25 are inherent in the Sato teachings.

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. ***See In re King***, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and ***Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.***, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). "Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention." ***RCA Corp. v. Applied Digital Data Systems, Inc.***, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.), *cert. dismissed*,

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468 U.S. 1228 (1984), citing **Kalman v. Kimberly-Clark Corp.**, 713 F.2d 760, 772 218 USPQ 781, 789 (Fed. Cir. 1983). The prior art disclosure need not be expressed in order to anticipate.

Standard Havens Products Inc. v. Gencor Industries Inc., 953 F.2d 1360, 1369, 21 USPQ2d 1321, 1328 (Fed.Cir. 1992).

Under the principles of inherency, we find that Sato teaches "a shaped conductive layer formed by etching ... with the lower portion having a faster etch rate as compared with an etch rate of the upper portion under the same etching conditions" as recited in Appellants' claim 25. Sato teaches on page 2 a T-shaped gate electrode is made of a single layer structure consisting of polycrystalline silicon. Sato teaches on page 3 that the method of manufacture includes a single step, step 2, whereby the T-shape gate electrode is formed by etching such that the width of the gate electrode material is narrower at the lower portion on the substrate side than the upper portion of the gate electrode on the surface side. On page 9, Sato teaches that the T-shaped gate electrode is a single layer in which physical qualities or features of the upper portion and the lower portion are different. Sato teaches some examples of the differences such as particle shape meaning grain size or the concentration of the impurities. We note that these differences are the same

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differences that Appellants have disclosed in their specification. In addition, Sato teaches on page 9 that the T-shaped electrode is formed by plasma etching, the same etching process as disclosed by the Appellants.

We acknowledge that Sato does not teach in great detail how the T-shaped electrode is formed by a single step. However, Sato does teach the same material with the different physical feature that would have a different etch rate. Viewing the Sato teachings as whole, we find that Sato inherently teaches that "a shaped conductive layer formed by etching ... with the lower portion having a faster etch rate as compared with an etch rate of the upper portion under the same etching conditions" as recited in Appellants' claim 25.

In the alternative, we find that it would have been obvious to one of ordinary skill from the Sato teaching to provide "a shaped conductive layer formed by etching ... with the lower portion having a faster etch rate as compared with an etch rate of the upper portion under the same etching conditions" as recited in Appellants' claim 25. The Federal Circuit reasons in *In re Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1088-89, 37 USPQ2d 1237, 1239-40, that for the determination of obviousness, the court must answer whether one of

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ordinary skill in the art who sets out to solve the problem and who had before him in his workshop the prior art, would have been reasonably expected to use the solution that is claimed by the Appellants. In view of the Sato teaching of forming a single layer of polycrystalline silicon with the upper and lower portions of the layer having different physical features such as grain size or concentrations of impurities and then forming a T-shaped gate in a single step of etching, those skilled in the art would have been led to a "a shaped conductive layer formed by etching" as recited in Appellants' claim 25.

Furthermore, we find that Appellants' claim 25 recites a product by process. Our reviewing court states in ***In re Marosi***, 710 F.2d 799, 803, 218 USPQ 289, 292-93, (Fed. Cir. 1983)

that "[w]here a product-by-process claim is rejected over a prior art product that appears to be identical, although produced by a different process, the burden is upon the applicants to come forward with evidence establishing an unobvious difference between the claimed product and the prior art process." In ***In re Thorpe***, 777 F.2d 695, 697, 227 USPQ 964, 966 (Fed. Cir. 1985), our reviewing court also states "[i]f the product in a product-by-process claim is the same as or obvious from a product of the

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prior art, the claim is unpatentable even though the prior product was made by a different process."

On page 5 of the reply brief, Appellants argue that claim 25 recites etch rates that are physical properties of each portion of the shaped conductive layer. However, as shown above, we have found that the Examiner has met the burden that Sato either inherently teaches or that it would have been obvious to those skilled in the art in view of the Sato teachings to provide "a shaped conductive layer ... having a upper portion and a lower portion ... with the lower portion having a faster etch rate as compared with an etch rate of the upper portion under the same etching conditions" as recited in Appellants' claim 25. A prima facie case is a procedural tool which means not only that the evidence of the prior art would reasonably allow the conclusion the examiner seeks, but also that the prior art compels such a conclusion if the Appellants produce no evidence or argument to rebut it. *In re Spada*, 911 F.2d 705, 707 n.3, 15 USPQ2d 1655, 1657 n.3 (Fed. Cir. 1990).

On page 15 of the brief, Appellants argue that Sato fails to teach that the lower portion of the shaped conductive layer includes a section having tapered walls as recited in Appellants'

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claims 9 and 10. Upon a closer review of Sato, we fail to find that Sato teaches or suggests that the lower portion includes a section having tapered side walls. Sato only teaches that a silicon layer 5 is formed on the side walls of the gate electrode 3 shown in Figure 1c. Therefore, we will not sustain the rejection of claims 9 and 10 as being anticipated under 35 U.S.C. § 102 or unpatentable under 35 U.S.C. § 103.

Finally, claims 6, 8 through 10, 22, 24 and 25 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims 23, 26, 33 and 34 present in U.S. Patent No. 5,543,646. On page 2 of the supplemental reply brief, Appellants argue that the rejection is improper because the Examiner did not specify which claims of the co-pending application are employed in the rejection. The

Examiner responded to the supplemental reply brief with a letter, mailed July 3, 1995, which clarified that Appellants' claims 6, 8 through 10, 22, 24 and 25 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims 23, 26, 33 and 34 present

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in copending application, serial no. 07/787,912⁵.

In view of this clarification, we find that the Examiner has overcome Appellants' argument. We note that Appellants have chosen not to argue any of the specific limitations of Appellants' claims as a basis for patentability. We are not required to raise and/or consider such issues. As stated by our reviewing court in *In re Baxter Travenol Labs.*, 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991), "[i]t is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art." 37 CFR § 1.192(a) as amended at 58 Fed. Reg. 54510, Oct. 22, 1993, which was controlling at the time of Appellants filing the brief, states as follows:

The brief . . . must set forth the authorities and arguments on which the appellant will rely to maintain the appeal. Any arguments or authorities not included in the brief may be refused consideration by the Board of Patent Appeals and Interferences.

Also, 37 CFR § 1.192(c)(6)(iv) states:

For each rejection under 35 U.S.C. 103, the argument shall specify the errors in the rejection and, if appropriate, the specific limitations in the rejected claims which are not described in the prior art relied on in the rejection, and shall explain how such

⁵Now U.S. Patent No. 5,543,646 issued August 6, 1996. In view of the issuance of a patent the rejection is no longer characterized as a provisional rejection.

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limitations render the claimed subject matter unobvious over the prior art. If the rejection is based upon a combination of references, the argument shall explain why the references, taken as a whole, do not suggest the claimed subject matter, and shall include, as may be appropriate, an explanation of why features disclosed in one reference may not properly be combined with features disclosed in another reference. A general argument that all the limitations are not described in a single reference does not satisfy the requirements of this paragraph.

Thus, 37 CFR § 1.192 provides that this board is not under any greater burden than the court which is not under any burden to raise and/or consider such issues.

In view of the above, we affirm the Examiner's decision that Appellants' claims 6, 8 through 10, 22, 24 and 25 are properly rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over the claims 23, 26, 33 and 34 present in U.S. Patent No. 5,543,646. In addition, we affirm the Examiner's decision that Appellants' claims 6, 8, 22, 24 and 25 are properly rejected under 35 U.S.C. §§ 102 or 103, but we reverse the Examiner's decision that Appellants' claims 9 and 10 are properly rejected under 35 U.S.C. §§ 102 or 103. Accordingly, the Examiner's decision is affirmed.

No time period for taking any subsequent action in

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connection with this appeal may be extended under 37 CFR
§ 1.136(a).

AFFIRMED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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