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PAT. AND
BOARD OF PATENT APPEALS
AND INTERFERENCES

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIEP V. TRAN

Appeal No. 95-2014
Application 07/557,249¹

ON BRIEF

Before HAIRSTON, KRASS, and JERRY SMITH, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 16.

The disclosed invention relates to a DRAM sensing cell scheme which uses a charge injection circuit to place an associated charge on a pair of bit lines through parasitic

¹ Application for patent filed July 24, 1990.

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capacitors. The first bit line of the pair receives any charge from the memory cell whose state is to be sensed. Next a comparator compares the electrical states of the first bit line and the second bit line to determine the state of the memory cell.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A memory cell sensing scheme comprising:
 - at least one pair of bit lines;
 - a plurality of decoders capable of being coupled to said bit lines;
 - a pair of low power supply voltage rails selectively connected to said decoders;
 - a charge injection circuit connected to said pair of low power supply voltage rails; and
 - a comparator capable of being coupled to said at least one pair of bit lines.

The references relied on by the examiner are:

Craycraft et al. (Craycraft)	4,636,664	Jan. 13, 1987
Terayama	4,943,952	July 24, 1990 (filed Dec. 27, 1988)
Ali	5,016,216	May 14, 1991 (filed Oct. 17, 1988)

Sze, "Semiconductor Devices - Physics and Technology," Bell Telephone Laboratories, Inc., pages 43-44 (1985)

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Claims 1 through 16 stand rejected under the second paragraph of 35 U.S.C. § 112.

Claims 1 through 16 stand rejected under the first paragraph of 35 U.S.C. § 112.

Claims 9 through 11 and 13 through 15 stand rejected under 35 U.S.C. § 102 as being anticipated by the conventional operation of the conventional differential bit line DRAM with line equalization.

Claims 9 through 11 and 13 through 15 stand rejected under 35 U.S.C. § 102(a), (e) or (g) as being anticipated by Terayama.

Claims 9 through 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Terayama.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103 as being unpatentable over Ali or Craycraft.

Claims 3 through 8 stand rejected under 35 U.S.C. § 103 as being unpatentable over Ali or Craycraft in view of Terayama.

Reference is made to the brief and the answer for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the 35 U.S.C. § 112, second paragraph

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rejection of claims 1 through 16, reverse the 35 U.S.C. § 112, first paragraph rejection of claims 1 through 16, reverse the 35 U.S.C. § 102 rejections and reverse the 35 U.S.C. § 103 rejections.

Pages 3 through 4 of the answer assert that the use of the term charge injection circuit in the claims "is repugnant to the technology which has developed in the art." As discussed on pages 5 through 7 of the brief, the specification provides a detailed definition of "charge injection circuit." Appellant argues on page 7 of the brief as follows:

As set out ad infinitum above, not only are the terms "charge injection" and charge injecting defined and recited in claims 1 through 16 ("Hence, the term charge injection applies to this phenomenon since an associated charge is placed on the bit lines through parasitic capacitors C1 and C2 in connection with the drop in voltage on their capacitor plates" as set out at page 4, line 19 et seq. [seq] of this brief), but also they are explained in the specification in an example as well as in formula (equation 1 quoted above and additionally equation 2) for calculating the difference in injected charge between bit lines. Further, figures 3 and 4 of appellant's drawing illustrate charge injection circuits. "Charge injection" has been exhaustively explained.

A patentee is free to be his or her own lexicographer.

Fromson v. Advance Offset Plate, Inc., 720 F.2d 1565, 1569, 219 USPQ 1137, 1140 (Fed. Cir. 1983). Thus, a patentee "may use terms in a manner contrary to or inconsistent with one or more of

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their ordinary meanings." Hormone Research Foundation, Inc. v. Genentech, Inc., 904 F.2d 1558, 1563, 15 USPQ2d 1039, 1043 (Fed. Cir. 1990). "If the claims, read in light of the specifications, reasonably apprise those skilled in the art both of the utilization and scope of the invention, and if the language is as precise as the subject matter permits," then 35 U.S.C. § 112, second paragraph is satisfied. Shatterproof Glass Corp. v. Libbey-Owens Ford Co., 758 F.2d 613, 624, 225 USPQ 634, 641 (Fed. Cir. 1985) (citing Georgia-Pacific Corp. v. United States Plywood Corp., 258 F.2d 124, 136, 118 USPQ 122, 132 (2d Cir. 1958)). Here, although the appellant's use of the term "charge injection circuit" is inconsistent with its use in the nonanalogous art of carrier injection discussed in the Sze reference, the term is clearly defined in appellant's specification. Accordingly, the rejection under the second paragraph of 35 U.S.C. § 112 is reversed.

On page 4, the answer asserts that because the term "charge injection" refers only to the process of introducing excess carriers as evidenced by Sze, there is no "charge injection" disclosed in the specification and thus, the claims stand rejected under 35 U.S.C. § 112, first paragraph. As discussed supra, however, appellant has clearly defined and disclosed charge injection and charge injection circuits. Accordingly, the

rejection under the first paragraph of 35 U.S.C. § 112 is reversed.

The 35 U.S.C. § 102 rejection on page 6 of the answer is based on subject matter asserted by the examiner to be well known in the art. While we agree with the examiner's position on page 12 of the answer regarding the considerable breadth of the claims, the examiner's burden is to provide evidence of anticipation. The examiner's speculations, assertions and opinions, without further support, will not anticipate a patent claim under 35 U.S.C. § 102. Accordingly, the 35 U.S.C. § 102 rejection based on the same is reversed.

The 35 U.S.C. § 102 rejection of claims 9 through 11 and 13 through 15 as being anticipated by Terayama is discussed in the paragraph bridging pages 7 and 8 of the answer. After thorough review of the examiner's position and the Terayama reference, we do not agree that Terayama discloses the claimed injecting step. The examiner describes Terayama on page 7 of the answer as follows:

Terayama shows a voltage generator circuit 11', which generator can, as at Figure 4, provide zero, $\frac{1}{2}V_{cc}$, or a voltage somewhat less than $\frac{1}{2}V_{cc}$ to its output 12. This generator, shown at Figure 3, comprises a capacitor C_1' , transistor Q_6 and inverters 23,24. Typically such inverters 23, 24 will have a series connected CMOS pair connected to the capacitor.

We do not agree that Terayama's level adjustment circuit 11' can be fairly understood as "injecting charge" to either of the bit lines. As disclosed in column 1, lines 39 through 45, column 2, lines 13 through 19 and column 3, lines 29 through 37, the bit lines are provided with the amplified "1" (Vcc) and "0" (GND) levels, respectively, not by level adjustment circuit 11' but by the sense amplifier. The lines are then short-circuited and a balanced potential of $\frac{1}{2}$ Vcc results on the pair of bit lines. Column 4, lines 53 through 57 discloses that the balanced potential is then capacitively pulled down by the level adjustment circuit 11'. In light of Terayama's disclosure, level adjustment circuit 11' does not inject charge on the bit lines; rather it discharges charge on the bit lines. Every limitation in the claim must be given effect. In re Wilder, 429 F.2d 447, 166 USPQ 545 (CCPA 1970); In re Geerdes, 491 F.2d 1260, 180 USPQ 789 (CCPA 1974). Accordingly, the 35 U.S.C. § 102 rejection of claims 9 through 11 and 13 through 15 cannot be sustained.

The paragraph bridging pages 14 and 15 of the answer provides further discussion of the Terayama reference as follows:

...Terayama appears to show at detail 11' in Figure 3 a circuit which, if not identical to, is very similar to that disclosed by Appellant at his Figures 3 and 4. Certainly Terayama uses his circuit for apparently the

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same ends as Appellant, and thus, even if *Donaldson* is introduced, it is clearly "equivalent" to the circuit(s) disclosed by Appellant.

As discussed supra, Terayama's level adjustment circuit is not used to inject charge. Accordingly, the examiner's assertions of equivalency between level adjustment circuit 11' and appellant's charge injection circuit as shown in Figures 3 and 4 are unfounded and cannot be supported.

Claims 9 through 16 are alternatively rejected under 35 U.S.C. § 103 as being unpatentable over Terayama. See pages 7 and 8 of the answer. For the same reasons discussed supra, Terayama would not have suggested to the skilled artisan the use of a charge injection circuit without some suggestion in the prior art to do so. While we recognize the great breadth of the claims, none of the references applied by the examiner would have suggested the use of a charge injection circuit. The 35 U.S.C. § 103 rejection is reversed.

The paragraph bridging pages 6 and 7 of the answer sets forth the obviousness rejection of claims 1 and 2 as being unpatentable over Ali or Craycraft as follows:

In Ali the two "low power supply voltage rails" are the two source regions coming from the ODD decoder transistors. The "charge injection circuit," as it can be understood, can be ground voltage terminal, which is well known to receive and emit "charges." In Craycraft et al. at, for example, Figure 4

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transistors 47 and 48 can be considered to be part of the "decoders," and their source regions can each [sic, be] considered to be a "rail," with the "charge injection" again being the ground potential. Thus considered the claims are felt obvious over either of Ali or Craycraft et al.

We do not agree that a ground voltage terminal can be fairly interpreted as the claimed charge injection circuit. A ground terminal will not inject charges on either of the bit lines. It is impermissible to use the claims as "a blueprint drawn by the inventor" to provide the specific details of the claimed invention. Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138 227 USPQ 543, 547 (Fed. Cir. 1985).

In summary, the 35 U.S.C. § 102 and § 103 rejections of claims 1 through 16 are reversed because the references applied by the examiner do not suggest or disclose a charge injection circuit or injecting charge on one of a pair of bit lines.

DECISION

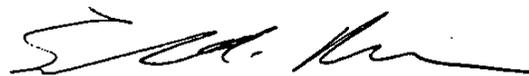
The decision of the examiner rejecting claims 1 through 16 under the first and second paragraphs of 35 U.S.C. § 112 is reversed, the decision of the examiner rejecting claims 9 through

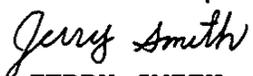
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11 and 13 through 15 under 35 U.S.C. § 102 is reversed, and the decision of the examiner rejecting claims 1 through 16 under 35 U.S.C. § 103 is reversed.

REVERSED


KENNETH W. HAIRSTON
Administrative Patent Judge)


ERROL A. KRASS
Administrative Patent Judge)


JERRY SMITH
Administrative Patent Judge)

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