

MAILED

JAN 24 1996

Paper No. 12

PATENT OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FULPS V. VERMEER
AND EDWARD C. KING

Appeal No. 95-1970
Application 07/752,702¹

ON BRIEF

Before KRASS, JERRY SMITH, and FLEMING, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 17, constituting all the claims in the application.

¹ Application for patent filed August 30, 1991.

95-1970

Appeal No. 95-1970
Application 07/752,702

OPINION

We will sustain the rejection of claims 1 through 5 and 13 through 17 under 35 U.S.C. § 103 but we will not sustain the rejection of claims 6 through 12 under 35 U.S.C. § 103.

While we agree with appellants that there is no teaching in Morgan of making a determination of whether or not to conduct interleaving based on stored memory bank size information, we do find such a suggestion in appellants' description of the prior art on page 1 of the instant specification. Therein, appellants admit that interleaving is a well known addressing technique which equally divides memory into two banks and stores data elements having successive addresses in alternate banks, thus permitting access of one bank while the other is being recharged.

The last two sentences of the second paragraph in the background section of the specification, at page 1, suggests that in order to employ interleaving, the relative sizes of the two banks must be the same.

Accordingly, appellants' own background section, i.e., prior art, clearly suggests that interleaving is advantageous and well-known and that the two memory banks on which the interleaving process is being effected must be of the same size. In our view, such knowledge, taken together with Morgan's teaching of registers holding memory size information for purposes of

Appeal No. 95-1970
Application 07/752,702

addressing would have led the artisan to employ such registers in order to determine relative sizes of memory and to use this information to determine whether an interleaving operation may be performed (where sizes are the same) or whether it may not be performed (where sizes are not the same). Broad independent claims 1, 13 and 14 require nothing more than this.

Claims 6 through 12 add the limitation of an "address router" for assigning bit positions to row and column addresses in response to the capacity of each bank stored in the register. We find no suggestion in Morgan or in the appellants' background section of the specification for such an "address router." While the examiner directs our attention to "columns 5-7" of Morgan for such a teaching, it is not clear to us exactly on what part of this large area of the patent the examiner places reliance. Morgan does mention at the top of column 7 that row and column address strobes are generated that activate corresponding banks in memory, but it is unclear to us why this should be considered an "address router," as claimed, wherein bit positions are assigned "in response to the capacity of each bank stored in the register."

We have sustained the rejection of claims 1 through 5 and 13 through 17 under 35 U.S.C. § 103 but we have not sustained the

Appeal No. 95-1970
Application 07/752,702

Douglas S. Foote
Intellectual Property Section
Law Department, NCR Corporation
World Headquarters
Dayton, OH 45479