

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIROYUKI YOSHIDA,
TAKAYUKI NIUYA,
TOSHIYUKI NAGATA
YOICHI MIYAI,
and YOSHIHIRO OGATA

Appeal No. 95-1555
Application 07/871,530¹

ON BRIEF

Before JERRY SMITH, FLEMING and TORCZON, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 10 through 21. Claims 1 through 9 have been canceled. Appellants' invention relates to a semiconductor integrated circuit for a dynamic random access memory (RAM) and a method for

¹ Application for patent filed April 21, 1992.

manufacturing it. Appellants disclose on pages 11 through 14 of the specification that Figure 1 is a first embodiment of a dynamic RAM memory cell. Appellants disclose on page 12 of the specification that the memory cell contains a p⁻-type substrate (81) and a highly concentrated p⁻-type semiconductor layer (80) formed over the p⁻-type substrate (81). Appellants disclose that the semiconductor layer (80) has a higher concentration than the p⁻-type substrate (81). Appellants' claims 10 through 15 are directed to this embodiment.

On pages 18 and 19 of the specification, Appellants disclose another embodiment of their invention as shown in Figure 18. Appellants disclose that the memory cell contains a n-type substrate (101) with a p⁻-type semiconductor layer (100) formed over the n-type substrate (101). In addition, a higher concentrated p-type semiconductor layer (80) is formed over the p⁻-type semiconductor layer (100). Appellants' claims 16 through 21 are directed to this second embodiment.

Independent claims 10 and 16 are reproduced as follows:

10. A semiconductor integrated circuit device comprising:
a semiconductor substrate of a first conductivity type;
a layer of semiconductor material of said first conductivity type but of increased dopant concentration in relation to said

Appeal No. 95-1555
Application 07/871,530

substrate overlying said substrate of said first conductivity type;

said layer of semiconductor material of said first conductivity type and said semiconductor substrate of said first conductivity type being provided with a vertical trench;

said vertical trench extending through said layer of semiconductor material of said first conductivity type and into said semiconductor substrate of said first conductivity type and bottoming within said semiconductor substrate of said first conductivity type;

a first liner of insulation material bounding the vertical trench;

a second liner of insulation material within the vertical trench and disposed in inwardly spaced relationship with respect to said first liner of insulation material;

first conductive material filling the portion of the vertical trench within said second liner of insulation material;

second conductive material filling the space in said vertical trench defined between said first and second liners of insulation material;

said first and second conductive materials and said second insulation liner defining a trench capacitor in which said first and second conductive materials are capacitor plates and the second liner of insulation material is a dielectric layer therebetween;

a field-effect transistor provided in said layer of semiconductor material of said first conductivity type and electrically connected to said trench capacitor;

said trench capacitor and said field-effect transistor defining a memory cell;

said field-effect transistor including spaced source and drain regions of a second conductivity type disposed in said

Appeal No. 95-1555
Application 07/871,530

layer of semiconductor material of said first conductivity type and opening onto the top surface thereof;

a portion of said layer of semiconductor material of said first conductivity type disposed between said source and drain regions of the second conductivity type defining a channel region;

a gate electrode of conductive material disposed above said channel region;

a layer of insulation material interposed between said gate electrode and said channel region and defining a gate insulator;

a region of the second conductivity type disposed in said layer of semiconductor material of said first conductivity type and extending between said source region and said second conductive material defining a capacitor plate of said trench capacitor to connect said field-effect transistor to said capacitor of said memory cell and comprising an annular dopant region of said second conductivity type bounding the upper portion of the vertical trench; and

the increased dopant concentration of said layer of semiconductor material of said first conductivity type in relation to said substrate of said first conductivity type limiting the growth of depletion layers to prevent linkage of the capacitor to a capacitor of an adjoining memory cell by the formation of a depletion layer extending toward the capacitor of the adjoining memory cell beyond an acceptable extent.

16. A semiconductor integrated circuit device comprising:

semiconductor substrate means including substrate components of at least a first conductivity type;

said semiconductor substrate means being provided with a vertical trench extending thereunto from the top surface thereof;

a first liner of insulation material bounding the vertical trench provided in said semiconductor substrate means;

Appeal No. 95-1555
Application 07/871,530

a second liner of insulation material within the vertical trench provided in said semiconductor substrate means and disposed in inwardly spaced relationship with respect to said first liner of insulation material;

first conductive material filling the portion of the vertical trench within said second liner of insulation material;

second conductive material filling the space in said vertical trench defined between said first and second liners of insulation material;

said first and second conductive materials and said second insulation liner defining a trench capacitor in which said first and second conductive materials are capacitor plates and the second liner of insulation material is a dielectric layer therebetween;

a field-effect transistor provided in said semiconductor substrate means and electrically connected to said trench capacitor; and

said trench capacitor and said field-effect transistor defining a memory, cell;

said semiconductor substrate means comprising:

a semiconductor substrate of the second conductivity type,

a buried semiconductor layer of the first conductivity type disposed on said semiconductor substrate of the second conductivity type, and

a second layer of semiconductor material of the first conductivity type and of increased dopant concentration in relation to said buried semiconductor layer of the first conductivity type disposed on said buried semiconductor layer of the first conductivity type and defining the top surface of said semiconductor substrate means;

Appeal No. 95-1555
Application 07/871,530

the vertical trench provided in said semiconductor substrate means extending through said second semiconductor layer of said first conductivity type and said buried semiconductor layer of said first conductivity type into said semiconductor substrate of said second conductivity type.

The references relied on by the Examiner are as follows:

Tsuchiya	4,922,313	May 1, 1990
Kumagai et al. (Kumagai)	5,041,887	Aug. 20, 1991 (filed May 14, 1990)
Anderson et al. (Anderson)	5,216,265	June 1, 1993 (filed Dec. 5, 1990)

Claims 10 through 15 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tsuchiya and Anderson. Claims 16 through 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tsuchiya and Kumagai.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the brief and the answer for the details thereof.

OPINION

After a careful review of the evidence before us, we agree with the Examiner that claims 10, 11, 14 and 15 are properly rejected under 35 U.S.C. § 103. Thus, we will sustain the rejection for these claims but we will reverse the rejection of the remaining claims on appeal for the reasons set forth *infra*.

At the outset, we note that Appellants have indicated on page 6 of the brief that the claims 10 through 21 do not stand or

Appeal No. 95-1555
Application 07/871,530

fall together. However, in the argument section of the brief, Appellants fail to point out reasons as to why the particular claim limitations for claims 11, 14 and 15 are further patentably distinguished over the applied art. For these claims, Appellants rely on the limitations as recited in Appellants' claim 10. 37 CFR § 1.192 (c)(5) amended June 23, 1988 states:

For each ground of rejection which appellant contests and which applies to more than one claim, it will be presumed that the rejected claims stand or fall together unless there is a statement otherwise, and in the appropriate part or parts of the arguments under subparagraph (c)(6) of this section appellant presents reasons as to why appellant considers the rejected claims to be separately patentable.

As per 37 CFR § 1.192 (c)(5) amended June 23, 1988, which was controlling at the time of Appellants' filing the brief, we will, thereby, consider Appellants' claims 10, 11, 14 and 15 to stand or fall together, with claim 10 being considered the representative claim.

In regard to the rejection of claims 10, 11, 14 and 15 under 35 U.S.C. § 103 as being unpatentable over Tsuchiya and Anderson, we note that only the limitation that is in dispute is "a layer of semiconductor material of said first conductivity type but of increased dopant concentration in relation to said substrate overlying said substrate of said first conductivity type" as

Appeal No. 95-1555
Application 07/871,530

recited in Appellants' claim 10. On pages 6 and 7 of the brief, Appellants only argue that Tsuchiya fails to teach this limitation. Since this limitation is the only limitation argued that distinguishes Tsuchiya, we find that Tsuchiya teaches all the other limitations of claim 10.

The Examiner notes on page 2 of the final action that Tsuchiya teaches all of the claimed limitations in Figure 12 except Tsuchiya does not show "a layer of semiconductor material of said first conductivity type but of increased dopant concentration in relation to said substrate overlying said substrate of said first conductivity type" as recited in Appellants' claim 10. However, the Examiner argues that Anderson teaches in Figure 2, item 40, this limitation. The Examiner argues that it would have been obvious to modify the Tsuchiya semiconductor integrated circuit device to include the Anderson's layer of semiconductor material of said first conductivity type (item 40 shown in Figure 2) but of increased dopant concentration in relation to said substrate overlying said substrate of said first conductivity type.

We note that Appellants do not argue that Anderson does not teach "a layer of semiconductor material of said first conductivity type but of increased dopant concentration in

Appeal No. 95-1555
Application 07/871,530

relation to said substrate overlying said substrate of said first conductivity type" as recited in Appellants' claim 10. Thus, we find that Anderson does teach this limitation. However, Appellants do argue on pages 7 and 8 of the brief that the proposed combination of Tsuchiya and Anderson relied upon by the Examiner for the purpose of the rejection of claims 10 through 15 is based upon directions from Appellants' disclosure, rather than suggestions contained in the references themselves. Thus, the only question before us is whether there are reasonable teachings or suggestions found in the prior art for modifying the Tsuchiya integrated circuit device with a layer of semiconductor material of said first conductivity type but of increased dopant concentration in relation to said substrate overlying the substrate of said first conductivity type as recited in Appellants' claim 10.

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). In addition, the Federal Circuit states that "[t]he mere fact that

Appeal No. 95-1555
Application 07/871,530

the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." **In re Fritch**, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), **citing In re Gordon**, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

"Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." **Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.**, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), **citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.**, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), **cert. denied**, 469 U.S. 851 (1984). In addition, the Federal Circuit reasons in **Para-Ordnance Mfg v. SGS Importers International**, 73 F.3d at 1087-88, 37 USPQ2d at 1239-40, that for the determination of obviousness, the court must answer whether one of ordinary skill in the art who sets to solve the problem, and who had before him in his workshop the prior art, would have been reasonably expected to use the solution that is claimed by the Appellants.

Appeal No. 95-1555
Application 07/871,530

To answer this question, we first must determine what the prior art places before the skilled artisan in his workshop. Anderson teaches in column 1, lines 39-47, that for DRAMs of the trench capacitor type, engineers have observed a problem in which leakage current flows through the upper portion of the storage node near the top of the trench into the silicon substrate. Anderson states in column 1, lines 48-51, that it is the object of their invention to provide a process which will eliminate undesirable leakage current near the top of the trench for trench capacitor type high density dynamic random access memories. Anderson further teaches in column 1, lines 57-68, a method of reducing gate diode leakage in trench type capacitor type dynamic random access memory devices. Anderson teaches that the storage node of the capacitor is formed by placing a storage node material, such as arsenic, into the trench walls of the device at a first tilt and a second tilt. The angle of the second tilt is higher than the angle of the first tilt. This higher angle provides the storage node with a larger concentration of doping around the upper portion of the trench walls. This larger concentration of doping reduces the charge leaking for the upper portion of the storage node into the substrate of the semiconductor material.

In column 3, lines 15-28, Anderson further teaches that Figures 2 and 3 shows the trench capacitors 16a and 16b extend through P-tank 40 into the P substrate 48. Anderson further teaches that on the outside of the trench capacitor walls, the storage node material, arsenic, is implanted creating an implanted arsenic layer 50. The arsenic layer 50 creates the N+ storage node of the trench capacitors. The upper portion of the storage node on the top of the trench edge where the leakage current could flow into the P-tank 40 is indicated by reference numeral 51. Anderson teaches in column 3, lines 50-61, that the P-tank 40 is implanted by an increased dopant over the p type substrate 48. Anderson teaches that the purpose of the increased dopant p-tank layer 40 is to control trench capacitance leakage and latchup.

Tsuchiya is also concerned with trench capacitor type high density dynamic random access memories. Thus, Tsuchiya's trench capacitor type high density dynamic random access memories are subject to the same problems recognized by Anderson.

Those skilled in the art having both the teachings of Tsuchiya and Anderson before them would have recognized from the teachings of Anderson that it would have been desirable to use the Anderson method of doping of the storage node and the

Appeal No. 95-1555
Application 07/871,530

increased dopant p layer in the Tsuchiya's trench capacitor type dynamic random access memory. Furthermore, those skilled in the art would have had reason to make the modification for reducing leakage current and trench capacitance leakage as well as to control latch up. Therefore, we find that it would have been obvious to one skilled in the art to modify Tsuchiya by providing the Anderson increased dopant in relation to the substrate as recited in claims 10, 11, 14 and 15.

Turning to the Examiner's rejection of Appellants' claim 12, Appellants argue on page 9 of the brief that neither Tsuchiya nor Anderson teach or suggest "the depth of said layer of semiconductor material of said first conductivity type as defined by its boundary with said substrate of said first conductivity type is located at substantially the middle depth position of the vertical trench" as recited in claim 12. The Examiner has not responded to this argument. After a careful review of Anderson and Tsuchiya, we find that these references fail to teach or suggest this limitation and thereby we will not sustain the Examiner's rejection of claim 12 as well as claim 13 which depends from claim 12.

Appeal No. 95-1555
Application 07/871,530

The Examiner also has rejected claims 16 through 21 under 35 U.S.C. § 103 as being unpatentable over Tsuchiya and Kumagai. On page 11 of the brief, Appellants argue that neither Tsuchiya or Kumagai teaches or suggests "a buried semiconductor layer of the first conductivity type disposed on said semiconductor substrate of the second conductivity type" as recited in claim 16. The Examiner argues in the final action that the lower portion of the layer 3 of Kumagai meets this limitation because it is a diffuse region.

After a careful review of Kumagai, we fail to find that the lower portion of the Kumagai layer 3 meets a buried semiconductor layer as recited in Appellants' claim 16. Appellants argue on page 12 of the brief that claim 16 is directed to the embodiment shown in Figure 18 of the Appellants' drawing which shows a distinct layer 100. We fail to find that Kumagai teaches a buried layer as recited in Appellants' claim 16 and thereby we will not sustain the Examiner rejection of claim 16 as well as claims 17 through 21 that depend from claim 16.

In view of the foregoing, the decision of the Examiner rejecting claims 10, 11, 14 and 15 under 35 U.S.C. § 103 is affirmed; however, the decision of the Examiner rejecting claims 12, 13 and 16 through 21 under 35 U.S.C. § 103 is reversed.

Appeal No. 95-1555
Application 07/871,530

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR 1.136(a).

AFFIRMED-IN-PART

JERRY SMITH)	
Administrative Patent Judge)	
)	
)	
)	
MICHAEL R. FLEMING)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS
)	AND
)	INTERFERENCES
)	
RICHARD TORCZON)	
Administrative Patent Judge)	
)	

Appeal No. 95-1555
Application 07/871,530

TEXAS INSTRUMENTS INCORP.
WILLIAM E. HILLER
P.O. BOX 655474
M/S 219
DALLAS, TX 75265