

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES  
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*Ex parte* MASAYUKI MIYABAYASHI

Appeal No. 95-1527  
Application No. 07/862,066<sup>1</sup>  
\_\_\_\_\_

HEARD: October 16, 1997  
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Before THOMAS, JERRY SMITH, and CARMICHAEL, *Administrative Patent Judges*.

CARMICHAEL, *Administrative Patent Judge*.

*DECISION ON APPEAL*

This is an appeal from the final rejection of Claim 1, which constitutes the only claim in the application.

We affirm.

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<sup>1</sup> Application for patent filed April 2, 1992.

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Appellant's Claim 1 is reproduced as follows:

1. A read-out circuit for use with a semiconductor memory device, said read-out circuit comprising:

first selecting means for selectively reading at least one datum from a plurality of memory means;

first data storing means for storing the data read out by said selecting means;

transferring means for transferring the data stored in said first data storing means in synchronism with an external clock signal;

second data storing means for storing the data transferred from said transferring means;

second selecting means for selectively outputting to an output port the data stored in said second data storing means; and

presetting means for presetting the voltage level of the line onto which said first selecting means reads out data.

The Examiner's Answer relies on admitted prior art and the following prior art reference:

Lam et al. (Lam)	4,731,758	Mar. 15,
1988		

**OPINION**

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Claim 1 stands rejected under 35 U.S.C. § 103 as unpatentable over admitted prior art in view of Lam.

The admitted prior art is illustrated in Figure 7 and described on pages 1-3 of Appellant's Specification. According to the examiner, it would have been obvious to modify the admitted prior art by incorporating the recited presetting means in order to provide high access speed as taught by Lam. Examiner's Answer at 3. Appellants argue that Lam fails to deal with the problem of increased capacitance as a result of the selection arrangement and also fails to suggest any means of solving that problem. Appeal Brief at 4-5.

We agree with the examiner.

The only difference between the admitted prior art and the claimed invention is that the claimed invention adds a presetting means. Specification at 7, lines 3-5. The Specification discloses a pre-charging transistor as a presetting means. Specification at 9, lines 17-21.

Lam also discloses a pre-charging transistor as a presetting means in a read-out circuit for use with a semiconductor memory device. Column 5, line 65, through column 6, line 9. Lam suggests such an arrangement in order

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to increase access speed to the memory. Column 8, lines 59-64. Thus, Lam motivated one of skill in the art to add a pre-charging transistor as a presetting means in Figure 7's prior art read-out circuit.

Because Lam suggested the modification to the admitted prior art in order to obtain fast memory access, the claimed invention would have been obvious. It does not matter whether the prior art motivation is the same as Appellant's motivation as argued by Appellant. Lam's suggestion is clearly applicable to an arrangement with the conventional selection means shown in Figure 7.

Appellant argues that Lam lacks the recited first selection means. Appeal Brief at 4. We fail to see how such a lack would vitiate Lam's suggestion to precharge the output of the conventional selection means shown in Figure 7.

Moreover, we disagree with Appellant's argument. Lam discloses the recited first selection means. Column 5, lines 15-23. Lam's presetting means (precharge transistor 78) presets the output of Lam's selecting means (word line select transistor 74) just as in Appellant's invention. We see no

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difference between Lam's disclosure and the subject matter of

Claim 1. Lam's read-out circuit in Figure 2 includes:

first selecting means (word line select transistor  
74);

first data storing means (latch 92/94/96/98);

transferring means (transfer gate 148);

second data storing means (latch 126/128/130/132);

second selecting means (transfer gate 150); and

presetting means (precharge transistor 78).

Those means as disclosed by Lam fully perform all the recited functions and are equivalent to Appellant's disclosed means which include:

first selecting means (word or column select  
transistor Qc);

first data storing means (latch F.F.D.);

transferring means (transfer gate Qt);

second data storing means (latch F.F.S.);

second selecting means (transfer gate Qy); and

presetting means (precharge transistor Qp).

Because Lam fully discloses the claimed invention, we cannot agree with Appellant's argument that Lam lacks the recited first selection means in the claimed combination.

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***CONCLUSION***

The rejection of Claim 1 under 35 U.S.C. § 103 as unpatentable over admitted prior art in view of Lam is sustained.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

**AFFIRMED**

JAMES D. THOMAS	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
JERRY SMITH	)	)
Administrative Patent Judge	)	APPEALS AND
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	)	
JAMES T. CARMICHAEL	)	
Administrative Patent Judge	)	

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