

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GIULIO MAROTTA
and EROS PASERO

Appeal No. 95-1017
Application 07/828,063¹

ON BRIEF

MAILED

FEB 24 1997

PAT. & T.M. OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Before THOMAS, JERRY SMITH and FLEMING, *Administrative Patent Judges*.

FLEMING, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 6 and 7.² Claim 8 has been allowed. Claims 1 through 5 have been canceled.

¹ Application for patent filed January 30, 1992.

² On page 1 of the final action, dated July 2, 1993, the Examiner states that claims 6 and 7 are objected to. However, on page 2 of the final action, claims 6 and 7 are rejected under 35 U.S.C. § 103. Furthermore, Appellants' brief on page 1 states that the status of claims 6 and 7 are finally rejected. Thus, we view page 1 of the final action as an error and the Examiner intended to state that claims 6 and 7 are rejected.

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The invention generally relates to electronic circuits that are named neural nets because of their functional likeness to the tridimensional physiological structures of cerebral neurons. On page 3 of the specification, Appellants disclose that it is known that the nerve cells of the brain are arranged in a complex tridimensional mat that interacts through particular regions named synapses. The passage of the nerve stimulus from neuron to neuron takes place through the synapses.

Appellants disclose on page 9 of the specification that Figure 2 shows a circuit diagram of a voltage-current converter for forming a synapse according to their invention and Figure 3 shows a diagram comprising two synapses converging to a neuron. On page 11 of the specification, Appellants disclose that Figure 2 is able to provide a positive or negative output current I_{OUT} proportionally equal to the difference between V_{IN} and V_w .

On page 13 of the specification, Appellants disclose that Figure 3 shows the assembly of two synapses of Figure 2 connected in series and converging to a neuron realized as a differential amplifier. The differential amplifier having an output providing a current equal to the algebraic sum of the respective I_{OUT} currents provided by each of the synapses.

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The independent claim 6 is reproduced as follows:

6. An integrated circuit in the form of cells of MOS transistors for converting a voltage into a current in forming synapses of a neural network, said integrated circuit comprising:

a plurality of individual MOS transistor cells connected in series to form a set of synapses of a neural nucleus, each of said MOS transistor cells including

a first MOS transistor serving as a current generator,

first and second parallel branches connected at one end at a first node to said first MOS transistor,

second and third MOS transistors respectively disposed in said first and second branches and connected together in a push-pull configuration,

an input voltage terminal connected to the gate of said second MOS transistor in said first branch,

a weighting voltage terminal connected to the gate of said third MOS transistor in said second branch,

fourth and fifth MOS transistors respectively disposed in said first and second branches and serially connected to said second MOS transistor and said third MOS transistor respectively, said fourth and fifth MOS transistors having their gates connected together,

said fourth MOS transistor having its gate connected to a second node disposed in the connection between said fourth MOS transistor and said second MOS transistor such that said fourth MOS transistor is connected as a diode,

a capacitor connected between the gate of said third MOS transistor included in said second branch and said weighting voltage terminal for storing the voltage for weighting the synapse, and

a third node connected between said third MOS transistor and said fifth MOS transistor included in said second branch for drawing output current and defining the output node for the respective MOS transistor cell;

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the output nodes of each of said plurality of MOS transistor cells being directly connected to each other in forming the set of synapses of a neural nucleus; and

a differential amplifier having first and second inputs, the first input of said differential amplifier being connected to the output from said output nodes of said plurality of MOS transistor cells and the second input of said differential amplifier being connected to ground;

said differential amplifier having an output providing a current as the algebraic sum of the respective currents provided by each of the plurality of synapses as defined by the respective MOS transistor cells.

The Examiner relies on the following references:

Lish	4,866,645	Sep. 12, 1989
Leivian et al. (Leivian)	5,097,141	Mar. 17, 1992

Claims 6 and 7 stand rejected under 35 U.S.C. § 103 as being unpatentable over Leivian and Lish.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs³ and answer for the respective details thereof.

³ Appellants filed an appeal brief on April 4, 1994. We will reference this appeal brief as simply the brief. Appellants filed a reply brief on July 25, 1994. The Examiner responded to the arguments of the reply brief in the Examiner's letter dated August 24, 1994. Because the Examiner has responded to the arguments of the reply brief, we find the reply brief as being entered and considered by the Examiner.

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OPINION

We will not sustain the rejection of claims 6 through 7 under 35 U.S.C. § 103.

The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), citing *W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

Appellants argue on page 5 of the brief and page 2 of the reply brief that there is no suggestion in either Leivian or Lish for modifying Leivian in the manner proposed by the Examiner. Appellants point out that the Examiner proposes to modify Leivian's circuit shown in Figure 7 by removing the respective current mirrors, elements 138, 158, 160, 164, 138 and 166, and

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the differential amplifier, elements 130, 132, 134, 136, and 138. In other words, the Examiner proposes to use only the differential amplifier, elements 138, 146, 148, 150, 152 and 154, of the Leivian circuit shown in Figure 7.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), citing *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." *Para-Ordnance Mfg. v. SGS Importers Int'l*, 73 F.3d at 1087, 37 USPQ2d at 1239, citing *W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

The Examiner fails to show that the prior art suggests the desirability of the modification proposed by the Examiner to the Leivian circuit shown in Figure 7. However, the Examiner does argue that *In re Porter*, 68 F.2d 971, 20 USPQ 298 (CCPA 1934) establishes obviousness. On page 5 of the answer, the Examiner sets forth the following:

As stated in *In re Porter*, 20 USPQ 298, "if the omission of an element is attended by a corresponding omission of the function performed by that element,

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there is no invention if the elements retained perform the same functions as before." See also In re Kuhle, 188 USPQ 7.

The Examiner does not provide us with any analysis as to how the facts in the record support the Examiner's legal conclusion of obviousness. "[I]t is facts appearing in the record, rather than prior decisions in and of themselves, which must support the legal conclusion of obviousness under 35 U.S.C. 103." *In re Cofer*, 354 F.2d 664, 667, 148 USPQ 268, 271 (CCPA 1966).

As pointed out above, the Examiner has the burden to establish that the prior art suggests to those skilled in the art the modification proposed by the Examiner. Neither Leivian nor Lish suggests that it is desirable to only use the differential amplifier formed by transistors 146-154 as an artificial synapse in an artificial neuron.

Leivian teaches in column 7, line 30, through column 8, line 25, that Figure 6 discloses an analog embodiment of an artificial neuron 100 that uses a plurality of comparators 102, 104 and 106 responsive to the input signal vector and the weight signals for providing the output signal of the neuron as the absolute value of the difference between the respective input signal vectors and the weight signals. In column 8, lines 25-29, Leivian states that Figure 7 is a more detailed description of the absolute value comparator 102 shown in Figure 6.

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Leivian teaches in column 8, lines 25-65, that the purpose of the absolute value comparator 102 shown in Figure 7 is to provide an absolute current value of the difference of the voltage of the input signal V_{IN1} and the voltage of the weight signal V_{W1} . Leivian teaches in column 8, lines 17-38, the operation of the differential amplifier circuits, 130-140 and 146-154, and the current mirror circuits, 158-160 and 164-166. There Leivian discloses that the purpose of comparator 102 is to provide current I_{102} which always has a positive value and negative slope when the difference $V_{IN1}-V_{W1}$ is negative and a positive value and positive slope when the difference $V_{IN1}-V_{W1}$ is positive. Leivian shows this relationship graphically in Figure 8.

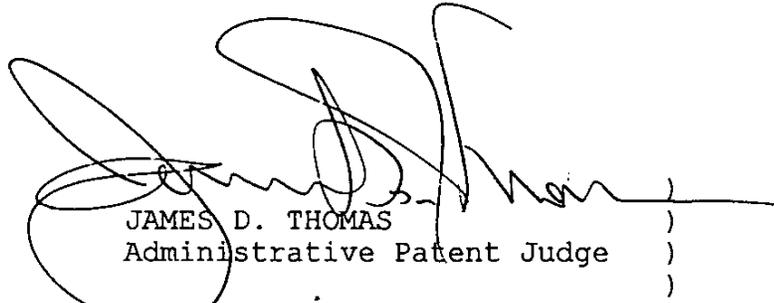
Furthermore, we note that to only use one of the Leivian differential amplifiers would not provide an absolute value of the difference, but only provide the difference. Appellants, on the other hand, disclose that the purpose of their circuit is to provide the difference. We fail to find any suggestion in Leivian or Lish to those skilled in the art that it would have been desirable to have an artificial neuron based upon the difference of the signal voltage and the synapse weight signal and thereby suggest modifying the Leivian absolute value comparator 102 shown in Figure 2 to provide a simple difference comparator.

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Since there is no evidence in the record that the prior art suggested the desirability of such a modification, we will not sustain the Examiner's rejection of claims 6 and 7.

We have not sustained the rejection of claims 6 and 7 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

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JAMES D. THOMAS)	
Administrative Patent Judge)	
)	
JERRY SMITH)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
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