

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT DOV HERZL and
DAVID A. SCHROTER

Appeal No. 95-0692
Application 07/755,237¹

ON BRIEF

Before THOMAS, FLEMING and CARMICHAEL, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed September 5, 1991.

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Application 07/755,237

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 6, which constitute all the claims remaining in the application.

Representative claim 4 is reproduced below:

4. Apparatus for reserving a bus for data transfer in a multi-processor data processing system containing a plurality of data buses interconnecting a plurality of storage control elements, wherein each of said storage control elements is assigned a default data bus, said apparatus comprising:

token control logic means for passing a token from one storage control element to another upon an occurrence of a machine cycle; and

priority logic means for detecting a request for data transfer from one of said storage control elements, said one of said storage control elements being a requesting source, said priority logic means reserving said requesting source's default data bus for said requested data transfer when all of said plurality of data buses are not available until said token is passed to said requesting source and at least one of said data buses is available, said priority logic means including means for avoiding a conflict between data buses,

wherein data to be transferred from one storage control element to a second storage control element of said plurality of storage control elements spends at least one machine cycle in a data bus being used for the data transfer, and

wherein said priority logic means upon receipt of said token by the requesting source, attempts to first reserve the requesting source's default data bus, but if the default data bus is not available, said priority logic means then attempts to reserve an alternate data bus.

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The following references are relied on by the examiner:²

Boudreau et al. (Boudreau)	4,654,788	Mar. 31, 1987
Eikill et al. (Eikill)	5,131,085	Jul. 14, 1992
		(Filed Dec. 4, 1989)

Claims 1 to 6 stand rejected under 35 U.S.C. § 103.³ As evidence of obviousness, the examiner relies upon Boudreau in view of Eikill.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and the answer for the respective details thereof.⁴

² The other two references listed at the top of page 3 of the answer have not been considered by us since, as noted by the examiner, they have not been relied upon in any rejection of any claim on appeal.

³ The bottom of the first page of the examiner's answer indicates that the examiner has permitted entry of the amendment filed with the brief.

⁴ The outstanding objection to the drawings under 37 CFR § 1.83(a) is a petitionable rather than appealable matter. We note in passing, however, that we disagree with the examiner's observation at page 8 of the answer that Fig. 3 does not provide a means for avoiding conflict. The referenced description in the paragraph bridging pages 12 and 13 of the specification as filed does, in our view, convey the conflict avoidance concept, but it appears that it may be more clearly depicted in the Fig. 3 version by modifications to the various arrows intercommunicating the priority logic units 91 and 92 to be more consistent with the verbal description just noted at pages 12 and 13 of the specification.

OPINION

As a result of our thorough study of the combined teachings and suggestions of Boudreau and Eikill, we must reverse the outstanding rejection of all claims on appeal under 35 U.S.C.

§ 103.

Despite the examiner's attempt to correlate the various teachings of the references in the statement of the rejection at pages 3 through 5 of the answer as to the claims on appeal, the relevance of each reference to the particular claim language recited in independent claims 1 and 4 on appeal is hard to determine individually, let alone collectively, as argued by the examiner. Even in view of Boudreau's teaching in the paragraph bridging cols. 31 and 32 that it may be possible to use other types of priority resolution and timing circuits than those disclosed in his patent, we find that the artisan would not have found it obvious to have utilized the grant token line 76 as well as the various select token lines of each slave device connected to each master device of Eikill in Boudreau.

Page 4 of the answer asserts that Boudreau did not specifically disclose the requesting source attempting to reserve a bus. The examiner appears to find this feature obvious alone in light of Boudreau's priority resolver logic circuits and timing generation circuits 21 in Fig. 1 and discussed beginning in the middle of column 5. However, not only does this reasoning of the examiner appear to be based upon prohibited hindsight, it also fails simply because the corresponding priority resolver logic circuits of Boudreau do not teach or suggest such a reservation or attempt to reserve in Boudreau. On the other hand, Eikill's ability to transfer control of its working data bus prior to its use by next devices looks similar to an attempt to reserve a bus when a currently controlling device reaches the final cycle of its operation, that is, its transmission of working data, this device activates the grant token to indicate to all the other connected devices that the currently controlling device is on its final cycle of operation, thus freeing the interface for the following cycle. Eikill, col. 4, lines 12 to 14 and the discussion beginning at col. 6, line 11.

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Finally, the examiner's attempt to correlate certain language of representative independent claims 1 and 4 on appeal to the specific teachings of each reference fails to convince us of a proper correlation. With respect to the claimed priority logical functions, as in the representative independent claim 4 above, this logic means can reserve its own requesting source's default data bus for request of data transfer only when all of the plurality of data buses are available. Otherwise, such is stated to be delayed if all of the plurality of data buses are not available, and such occurs only when the token is passed to the requesting device and at least one of the data buses does eventually become available. The end of each independent claim recites further that the priority logic means must, upon receipt of the token by the requesting source, attempt to first reserve the requesting source's default data bus, but, if such a default bus is not available, the priority logic means must then attempt to reserve an alternate data bus. We do not see all of these features to be reasonably taught or suggested to the artisan from both references relied upon within 35 U.S.C. § 103.

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In view of the foregoing, we reverse the rejection of
claims 1 to 6 under 35 U.S.C. § 103.

REVERSED

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JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
MICHAEL R. FLEMING)	
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
)	
JAMES T. CARMICHAEL))
Administrative Patent Judge)	

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