

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

MAILED

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

DEC 13 1995

Ex parte MICHAEL J. MILLER and JOHN R. MICK

PAT.&T.M. OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Appeal No. 94-3170
Application 07/629,285¹

ON BRIEF

Before GARY V. HARKCOM, *Vice Chief Administrative Patent Judge*,
and JERRY SMITH and FLEMING, *Administrative Patent Judges*.

FLEMING, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 3 through 8.

The invention is directed to testing of digital systems. Appellants disclose on pages 1 and 2 of Appellants' specification that one known technique for testing of digital systems is the Level Sensitive Scan Design (LSSD) technique.

¹ Application for patent filed December 18, 1990.

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Under LSSD, memory elements, such as registers or flip-flops, are serially connected to form a scan-path for scanning in test data and scanning out test results. Appellants further disclose an improved test structure wherein the number of dedicated pins is minimized by multiplexing the command and data in the serial data input and the serial data output pins. Appellants state that an example of such test structure is found in U.S. Patent 4,710,927 by Michael J. Miller. Appellants disclose that multiplexing commands and test data on the same serial input and output pins is time-consuming. Appellants' Figure 1 shows a test structure using one serial command input pin, one serial data input pin, one serial command output pin and one serial data output pin. On page 7 of the specification, Appellants disclose that data register 46 receives the clock input signal on lead 20 and a serial data input signal on lead 25 and provides a serial data output signal on lead 27. Appellants disclose on page 13 of the specification another embodiment of the invention shown in Figure 1 where the data register 46 is replaced by a number of data registers. Appellants' Figure 3 shows an example of a structure to replace data register 46 of Figure 1. Appellants' Figure 3 shows data registers 46a through 46d wherein the serial data input lead 25 is connected to the serial data input terminal of each of the data registers 46a through 46d. The serial output terminals of each of the data registers 46a through 46d are

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provided to multiplexer 160, which selects one serial data output signal among the serial data output signals of the data registers 46a-46d. Each of the registers 46a through 46d can be individually loaded with parallel input data from bus 142. In addition, each of the registers 46a through 46d when selected by multiplexer 165 outputs data in parallel to a bus 140.

Claim 3 is reproduced as follows:

3. A diagnostic circuit comprising:

a command input lead for receiving a first serial command signal;

a data input lead for receiving a first serial data signal;

a clock input lead for receiving a clock signal;

a control lead for receiving an external control signal, said external control signal having first and second states;

a command register coupled to receive said clock signal of said clock input lead, said external control signal of said control lead and said serial command signal of said command input lead, for shifting in said first serial command signal and shifting out serially a second serial command signal when said external control signal is at said first state, said second serial command signal representing the content of said command register delayed by a predetermined number of cycles of said clock signal, said command register also provides a number of command output signals in parallel, said command output signals being the current content of said command register;

a plurality of data registers, each coupled to receive said clock signal of said clock input lead and said first serial data signal of said data input lead, for shifting in said first serial data signal, and for providing as a serial output a second serial data signal, said second serial data signal being the content of said data register delayed by a predetermined number of cycles of said clock signal, each data register also receiving

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a number of data input signals in parallel, and provides a number of data output signals in parallel;

a command output lead coupled to receive said second serial command signal; and

means coupled to receive said second serial data signals for selecting and providing as output said second serial data signal from one of said plurality of data registers; and

a data output lead coupled to receive said selected second serial data signal.

The Examiner relies on the following references:

Miller	4,710,927	Dec. 01, 1987
Stewart et al. (Stewart)	4,947,357	Aug. 07, 1990
Anderson et al. (Anderson)	5,130,989	Jul. 14, 1992

Claims 3 through 6 stand rejected under 35 U.S.C. § 103 as unpatentable over Miller and Stewart. Claims 7 through 8 stand rejected under 35 U.S.C. § 103 as unpatentable over Miller and Anderson.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs and answer for the respective details thereof.

OPINION

After a careful review of the evidence before us, we agree with the Examiner that claims 3 through 6 are directed to subject matter that would have been obvious to one of ordinary skill in the art within the meaning of 35 U.S.C. § 103 as evidenced by Miller and Stewart.

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At the outset, we note that Appellants have not indicated whether claims 3 through 6 stand or fall separately or together. We also note that these claims are not argued independently. We will treat claim 3 as a representative claim for the claims. *In re Nielson*, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987); *In re Kaslow*, 707 F.2d 1366, 217 USPQ 1089 (Fed. Cir. 1983); *In re Wiseman*, 596 F.2d 1019, 201 USPQ 658 (CCPA 1979).

In the Appellants' brief, Appellants emphasize that Appellants' claim 3 sets forth "a plurality of data registers, each coupled to receive said clock signal of said clock input lead and said first serial data signal data signal of said data input lead ... each data register also receiving a number of data input signals in parallel, and provides a number of data output signals in parallel". Appellants argue that neither Miller nor Stewart teaches this limitation.

The Examiner argues on page 6 of the answer that Stewart teaches in Figures 1, 2, 3A, and 3B a plurality of scanable data registers 12a to 12n. The Examiner further argues on page 14 of the answer that Miller teaches a data register which receives a number of data input signals in parallel and provides a number of data output signals in parallel.

In reviewing Stewart, we find that Stewart does teach a plurality of scanable registers as recited in Appellants' claim

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3. Stewart teaches in column 8, lines 45-62, the functional circuitry of computer system 10 which is to be tested. Referring to Figure 1, the functional circuitry of the computer system 10 is distributed in a number N of printed circuit boards 12a through 12n. Referring to Figure 2, each printed circuit board 12a through 12n includes a number of M integrated circuits 14a through 14m. Referring to Figures 3A and 3B, each integrated circuit 14a-14m is configured under test into a scan register 20, 22 and 24. Thus, the system scan controller 26 in a test mode shown in Figure 1 views each printed circuit board as a scan register. Stewart teaches in column 10, lines 19-30 that the system scan controller 26 supplies serial scan chains to input SDI of the scan registers 12a through 12n and expects serial scan chains output from a selected one of the scan registers via output SDO. Therefore, we find that Stewart does teach a plurality of scanable registers as recited in Appellants' claim 3.

Furthermore, we find that Miller teaches a data register which receives a number of data input signals in parallel and provides a number of data output signals in parallel. Miller teaches in column 3, lines 30-50, that Figure 1 illustrates a diagnostic circuit for use in testing another circuit that is represented as a state register 12. In column 3, line 65, through column 4, line 10, Miller teaches a diagnostic

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circuit 10 having a command register 40, a command decoding circuit 42 and a data register 46. In column 5, lines 25-60, Miller teaches that the data register 46 includes a clock input, a serial data input for use with the clock input for shifting serial test data into register 46 and a serial data output for use with the clock input for shifting serial test data out of register 46. Miller further teaches that data register 46 includes a load input, a number of parallel data inputs for use with the load input for loading test data in parallel into the register 46 and a number of parallel data outputs for transmitting test data in parallel out of the register. Thus, we find that Miller does teach a data register that also receives a number of data input signals in parallel and provides a number of data output signals in parallel as recited in Appellants' claim 3. Therefore, we find that the combination of modifying the Miller data register to include a plurality of data registers and a means to select each of the registers as taught by Stewart would meet all of the limitations as recited in Appellants' claim 3.

Appellants argue that the present invention discloses a diagnostic circuit for use in testing any integrated circuit and is independent of the circuit under test. Appellants argue that the Stewart data registers are present in the circuit to be tested and not in the diagnostic circuit. However, the Examiner

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is not relying on Stewart for this teaching. As shown above, Miller teaches a data register in the diagnostic circuit. The Examiner is relying on Stewart for the teaching that a data register may be made up of a plurality of data registers in which one of the plurality may be selected.

Appellants' argument on page 2 of the reply brief that using the Examiner's rationale for combining the teachings of Stewart and Miller, the resulting combination would teach a diagnostic circuit having multiple data registers switching between scan chains which is not required by the Appellants' claims. However, the question is not whether the combination may provide more limitations than what is being claimed by the Appellants, but whether the combination reads on all of the limitations recited in Appellants' claims. As shown above, the combination does in fact meet all of the limitations recited in Appellants' claim 3.

In addition, the question is not whether the Stewart plurality of data registers may be bodily incorporated into the Miller diagnostic circuit. The test of obviousness is not whether features of a secondary reference may be bodily incorporated into the primary reference's structure, nor whether the claimed invention is expressly suggested in any one or all of the references; rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill

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in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Appellants further argue that the combination was not suggested by the references because Miller does not show multiplexing for multiple data registers. We note that the courts have held that a suggestion to use a teaching from a reference does not have to be a specific teaching of that reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. See *In re Preda*, 401 F.2d 825, 159 USPQ 342 (CCPA 1968); *In re Shepard*, 319 F.2d 194, 138 USPQ 148 (CCPA 1963); and *In re Sernaker*, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983).

The question before us is whether one of ordinary skill in the art would have had reason to modify the Miller data register by using Stewart's teachings of using a plurality of data registers in which one is selected to receive the output. We note that the Federal Circuit stated that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84, (Fed. Cir. 1992), *citing In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). However, from the teachings in both

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suggested the desirability of modifying the Miller data register by using a plurality of registers as taught by Stewart.

Miller teaches in column 1, lines 57-66, that for diagnostic purposes, it is suggested that an additional diagnostic circuit be employed for each of the registers in which the test data is to be inserted. Miller further teaches that the diagnostic circuit include a diagnostic register which has the same length as the register to be tested. Thus, Miller recognizes the advantage of using scan testing at the circuit level versus at the system level.

Stewart teaches in column 1, lines 45-55, that it is advantageous when using scan techniques to test the functional circuitry of integrated circuits. Stewart teaches that instead of providing the entire system as a scan shift register that each functional circuitry be tested by forming each functional circuitry as a single register to be tested. Thereby, a plurality of registers are formed in which only one output is selected. From this teaching, Stewart suggests to one of ordinary skill in the art that Miller's diagnostic register may achieve the advantages of testing a smaller scan array by forming a plurality of smaller size registers to be used in the scan testing. Therefore, the decision of the Examiner rejecting claims 3 through 8 under 35 U.S.C. § 103 as being unpatentable over Miller and Stewart is sustained.

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Claims 7 through 8 stand rejected under 35 U.S.C. § 103 as unpatentable over Miller and Anderson. Appellants argue that Anderson does not disclose a plurality of data registers, each of which receives serial data signals at its scan-in terminal and shifts the serial data signal out at its scan-out terminal as recited in claim 7. The Examiner argues on page 19 of the answer that this limitation is an obvious design choice.

Our reviewing court in *In re Kuhle*, 526 F.2d 553, 555, 188 USPQ 7, 9 (CCPA 1975), held that the test for design choice turns on whether the use of the arrangement solves a stated problem. On page 14 of Appellants' specification, Appellants teach that by providing multiple data registers in which each register receives serial data signals at its scan-in terminal and shifts the serial data signal out at its scan-out terminal, intermediate test data can be stored and allow bypass paths. Clearly, this feature is directed to solving the testing problems that arise from a large scan path by providing smaller scan segments and is critical to the Appellants' invention. We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a *prima facie* case. *In re Knapp-Monarch Co.*,

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196 F.2d 230, 232 132 USPQ 6, 8 (CCPA 1961); *In re Cofer*, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Therefore, we will not sustain the Examiner's rejection of claims 7 through 8 under 35 U.S.C. § 103 as unpatentable over Miller and Anderson.

In view of the foregoing, the decision of the Examiner rejecting claims 3 through 6 under 35 U.S.C. § 103 as being unpatentable over Miller and Stewart is sustained. However, we have not sustained the Examiner's rejection of claims 7 through 8 under 35 U.S.C. § 103 as unpatentable over Miller and Anderson. Accordingly, the decision of the Examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR 1.136(a).

AFFIRMED-IN-PART


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