

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GARY L. SWOBODA
and
PETER N. EHLIG

Appeal No. 94-3053
Application 07/832,661¹

ON BRIEF

¹ Application for patent filed February 4, 1992. According to appellants, the application is a continuation of Application 07/388,286, filed July 31, 1989, abandoned.

Appeal No. 94-3053
Application 07/832,661

Before HAIRSTON, BARRETT and FLEMING, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 2 through 17, 20 through 28, 31 through 35, 39, 40, 55, and 60 through 64. Claims 36 through 38, 56 through 59, 65 and 66 stand objected to as depending from a rejected claim. Claims 41, 46 through 48, 50 and 51 have been allowed.² Appellants state on page 2 of the brief that claims 1, 18, 19, 29, 30, 32 through 40, 42 through 45, 49, 52 through 54 and 62 through 66 have been cancelled. Therefore, claims 2 through 17, 20 through 28, 31, 55, 60 and 61 are properly before us for our consideration.

Appellants' invention relates to an electronic data processing device which utilizes a processor and a serial scan

² We note that the summary of action incorrectly states the status of the final rejection of the claims.

circuit to monitor another processor on a semiconductor chip. The serial scan circuit is used to set the invention's processor to particular predetermined conditions and then check the chip's

processor for the existence of such conditions. When a predetermined condition is met, the invention's processor controls the operation of the monitored processor.

Independent claim 55 is reproduced as follows:

55. A data processing device comprising:

a semiconductor chip;

an electronic processor on-chip;

an on-chip condition sensor connected to said electronic processor for analysis of the operations thereof, including means for recognizing the occurrence of a predetermined condition during real time operation of said electronic processor and means responsive to the recognition of said predetermined condition for applying a control input to said electronic processor during said real time operation thereof; and

a serial scan circuit connected to said on-chip condition sensor for inputting to said on-chip condition sensor control information which causes

Appeal No. 94-3053
Application 07/832,661

said on-chip condition sensor to assume a selected one of a plurality of sensing configurations.

The references relied on by the examiner are as

follows:

d'Angeac et al. (d'Angeac)	4,597,042	June 24, 1986
Poret et al. (Poret)	4,674,089	June 16, 1987
Hester et al. (Hester)	4,788,683	Nov. 29, 1988

Rodnay Zaks and Alexander Wolfe (Zaks), From Chips to Systems: An Introduction to Microcomputers, (1987).

We note that the Examiner has maintained the following rejections: claims 2, 11 through 15, 17 and 55 under 35 U.S.C. § 102(b) as being unpatentable over Hester; claims 3, 23 through 26 under 35 U.S.C. § 103 as being unpatentable over Hester and Poret; claims 4, 5 and 16 under 35 U.S.C. § 103 as being unpatentable over Hester and Zaks; and claims 6 through 10 and 27 under 35 U.S.C. § 103 as being unpatentable over Hester and d'Angeac. The Examiner also sets forth in the Examiner's answer three new grounds of rejection which are as follows: claims 20 through 22, 28, 31, 60 and 61 under 35 U.S.C. § 103 as being unpatentable over Hester; claims 8

Appeal No. 94-3053
Application 07/832,661

through 10 under 35 U.S.C. § 103 as being unpatentable over Hester, d'Angeac and Poret; and claims 28 and 31 under 35 U.S.C. § 103 as being unpatentable over Hester and Poret.

Therefore, claims 2, 11 through 15, 17 and 55 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Hester. Claims 20 through 22, 28, 31, 60 and 61 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hester. Claims 3, 23 through 26, 28 and 31 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hester and Poret. Claims 4, 5 and 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hester and Zaks. Claims 6 through 10 and 27 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hester and d'Angeac. Claims 8 through 10 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hester, d'Angeac and Poret.

Appeal No. 94-3053
Application 07/832,661

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the briefs³ and the answers⁴ for the details thereof.

OPINION

After a careful review of the evidence before us, we agree with the Examiner that: claims 2, 11 through 15, 17 and 55 are properly rejected under 35 U.S.C. § 102(b) over Hester; claims 20 through 22, 60 and 61 are properly rejected under 35 U.S.C. § 103 over Hester; claims 3 and 23 through 26 are properly rejected under 35 U.S.C. § 103 over Hester and Poret;

³ Appellants filed an appeal brief on October 28, 1993. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on June 6, 1994. We will refer to this reply appeal brief as the reply brief. The Examiner responded to the reply brief in the supplemental Examiner's answer, mailed June 12, 1996 and thereby has entered and con-sidered the reply brief.

⁴ The Examiner responded to the brief with an Examiner's answer, mailed January 11, 1994. We will refer to the Examiner's answer as simply the answer. The Examiner responded to the reply brief with a supplemental Examiner's answer, mailed June 12, 1996. We will refer to the supplemental Examiner's answer as simply the supplemental answer.

Appeal No. 94-3053
Application 07/832,661

and claims 4, 5 and 16 are properly rejected under 35 U.S.C. § 103 over Hester and Zaks. Thus, we will sustain the rejection of these claims. However, we will reverse the rejections of claims 6 through 10, 27, 28 and 31 for the reasons set forth *infra*.

At the outset, we note that Appellants have argued, on pages 4-7 of their brief and in the reply brief, the following groupings of claims:

- (1) claims 2, 11-15, 17, 55;
- (2) claims 20, 21, 60;
- (3) claims 23-26;

- (4) claims 4, 5, 16; and
- (5) claims 6-8.

37 CFR § 1.192(c)(5), amended October 22, 1993, which was controlling at the time of Appellants filing the brief, states:

For each ground of rejection which appellant contests and which applies to more than one claim, it will be presumed that the rejected claims stand or fall

Appeal No. 94-3053
Application 07/832,661

together unless a statement is included that the rejected claims do not stand or fall together, and in the appropriate part or parts of the argument under subparagraph (c)(6) of this section appellant presents reasons as to why appellant considers the rejected claims to be separately patentable.

As per 37 CFR § 1.192(c)(7), which was also controlling at the time of Appellants' filing the brief, we will, thereby, consider the claims in each above group to stand or fall together as a group, with the broadest claim deemed to be the representative claim for that group.

In addition, Appellants separately argue claims 3, 9, 10, 22, 27, 28, 31 and 61. Therefore, we treated each of these claims separately.

Group (1) - representative claim 55

Claim 55 stands rejected under 35 U.S.C. § 102(b) in view of Hester. It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. ***See In re King***, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and

Appeal No. 94-3053
Application 07/832,661

Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

"Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention."

RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.), **cert. dismissed**, 468 U.S. 1228 (1984), **citing Kalman v.**

Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983), **cert. denied**, 465 U.S. 1026 (1984).

Upon a review of the limitations recited in Appellants' claim 55, we find that Hester discloses "a data processing device" (at col. 1, lines 1-2), "an electronic processor on-[a

semiconductor] chip" (at col. 2, line 33), "an on-chip condition

Appeal No. 94-3053
Application 07/832,661

sensor connected to said electronic processor . . ." (at col. 2, lines 32-34), "means for recognizing the occurrence of a pre-determined condition during real time operation of said electronic processor" (at col. 3, lines 22-26), "means responsive to the recognition of said predetermined condition for applying a control input to said electronic processor . . ." (at col. 2, lines 50-61; col. 3, lines 26-37; col. 4, lines 4-7), and "a serial scan circuit connected to said on-chip condition sensor . . ." (at col. 2, lines 32-34).

On page 4 of the brief and page 2 of the reply brief, Appellants only argue that Hester fails to disclose the following limitations recited in claim 55:

an on-chip condition sensor . . . including . . . means responsive to the recognition of said predetermined condition [of the electronic processor under test] for applying a control input to said electronic processor during said real time operation thereof.

Appellants do not argue in their briefs that the above claim language should be interpreted any more narrowly than its

Appeal No. 94-3053
Application 07/832,661

ordinary meaning. We must therefore give this claim language its broadest reasonable interpretation. **See *In re Morris***, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); ***In re Zletz***, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

With respect to the above-argued claim language, Hester discloses "an on-chip condition sensor" by teaching that "support processor 26 attaches to the microprocessor 28 in the system under test through the LSSD scan strings 30a and 30b." Col. 2, lines 32-34. Hester also discloses a "means responsive to the recognition of said predetermined condition for applying a control input to said electronic processor" More specifically, the device of Hester has "predetermined conditions" by disclosing that "[a]n instruction compare address register" contains "the desired instruction . . . compare values." Col. 3, lines 22-26. As to the limitation of "responsive to . . . for applying a control input . . . ," Hester teaches that the condition sensor "include[s] the ability to examine and alter

Appeal No. 94-3053
Application 07/832,661

registers in the system microprocessor" (col. 2, lines 59-61)

and

"control[s] and examine[s] the contents of all facilities within the microprocessor" (col. 4, lines 6-7). Hester performs this alter/control function by using the desired instruction "to enable the stop-on-address function" of the microprocessor. Col. 3, lines 22-37. Thus, the claim language that Appellants argue for claim 55 is met by Hester. Accordingly, we will sustain the Examiner's rejection of claim 55 under 35 U.S.C. § 102(b) in view of Hester.

Aside from the above claim language for claim 55, Appellants have chosen not to argue any of the other specific limitations as a basis for patentability. As stated by our reviewing Court in *In re Baxter Travenol Labs.*, 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991), "[i]t is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art." 37 CFR § 1.192(a), as amended at 58 Fed. Reg. 54510, Oct. 22, 1993, which was

Appeal No. 94-3053
Application 07/832,661

controlling at the time of Appellants filing the brief, states
as follows:

The brief . . . must set forth the
authorities and arguments on which the
appellant will rely to maintain the appeal.
Any arguments or authorities not included
in the brief may be refused consideration
by the Board of Patent Appeals and
Interferences.

Also, 37 CFR § 1.192(c)(6)(iii) states:

For each rejection under 35 U.S.C. 102, the
argument shall specify the errors in the
rejection and why the rejected claims are
patentable under 35 U.S.C. 102, including
any specific limitations in the rejected
claims which are not described in the prior
art relied upon in the rejection.

Thus, 37 CFR § 1.192 provides that, just as the Court is not
under any burden to raise and/or consider issues not raised by
an appellant, this board is also not under any such burden and
declines to do so for this group of claims.

Group (2) - representative claim 60

Appeal No. 94-3053
Application 07/832,661

Claim 60 stands rejected under 35 U.S.C. § 103 in view of Hester. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 117 S.Ct. 80 (1996), ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

On page 2 of the reply brief and page 4 of the brief, Appellants only argue that Hester fails to teach the limitations recited here below:

Appeal No. 94-3053
Application 07/832,661

an on-chip condition sensor . . . including . . . means for stopping said electronic processor automatically upon occurrence of said predetermined condition.

Hester meets the above language by teaching that the support processor "include[s] the ability to examine and alter registers in the system microprocessor" (col. 2, lines 59-61) and "control[s] and examine[s] the contents of all facilities within the microprocessor [under test]" (col. 4, lines 6-7). Hester performs this alter/control function by having a "desired instruction" that is used "to enable the stop-on-address function" of the microprocessor. Col. 3, lines 22-37; col. 4, line 10. Thus, the claim language that Appellants argue with respect to claim 60 is met by Hester and since anticipation is the epitome of obviousness, *In re Fracalossi*, 681 F.2d 792, 794, 215 USPQ 569, 571 (CCPA 1982), we will sustain the Examiner's rejection of claim 60 under 35 U.S.C. § 103 in view of Hester.

Appeal No. 94-3053
Application 07/832,661

Aside from the above claim language for claim 60, Appellants have chosen not to argue any of the other specific limitations as a basis for patentability. 37 CFR § 1.192(c)(6)(iv) states:

For each rejection under 35 U.S.C. 103, the argument shall specify the errors in the rejection and, if appropriate, the specific limitations in the rejected claims which are not described in the prior art relied on in the rejection, and shall explain how such limitations render the claimed subject matter

unobvious over the prior art. If the rejection is based upon a combination of references, the argument shall explain why the references, taken as a whole, do not suggest the claimed subject matter, and shall include, as may be appropriate, an explanation of why features disclosed in one reference may not properly be combined with features disclosed in another reference. A general argument that all the limitations are not described in a single reference does not satisfy the requirements of this paragraph.

Just as our reviewing Court is not under any burden to raise and consider issues not raised by an Appellant, **Baxter**, 952 F.2d at 391, 21 USPQ2d at 1285, this board is also not under

Appeal No. 94-3053
Application 07/832,661

any such burden, 37 CFR § 1.192, and declines to look beyond that argued by Appellants in their brief in this case.

Group (3) - representative claim 23

Claim 23 stands rejected under 35 U.S.C. § 103 in view of Hester and Poret. The extent of Appellants' argument for this group is "[t]hese rejections of Claims 23-26 are traversed for the same reasons given above (in Argument Section A) with respect to Claim 60." Brief at page 5. Thus, since Appellants have not argued anything in addition to that which they argued for claim 60, the rejection of claim 23 is also sustained for the reasons set forth above for claim 60. This board declines to look beyond that which has been argued by Appellants. ***Baxter***, 952 F.2d at 391, 21 USPQ2d at 1285; 37 CFR § 1.192.

Group (4) - representative claim 4

Claim 4 stands rejected under 35 U.S.C. § 103 in view of Hester and Zaks. The extent of Appellants' argument

Appeal No. 94-3053
Application 07/832,661

for this group is "[t]hese rejections of Claims 4-5 and 16 are traversed for the same reasons given above (in Argument Section A) with respect to Claim 55." Brief at page 6. Thus, since Appellants have not argued anything in addition to that which they argued for claim 55, the rejection of claim 4 is also sustained for the reasons set forth above for claim 55. Again, this board declines to look beyond that which has been argued by Appellants. Baxter, 952 F.2d at 391, 21 USPQ2d at 1285; 37 CFR § 1.192.

Group (5) - representative claim 6

Claim 6 stands rejected under 35 U.S.C. § 103 in view of Hester and d'Angeac. Appellants argue that this rejection should be reversed because this claim recites that "said on-chip condition sensor includes . . . sensor circuit selection circuitry," and neither Hester nor D'Angeac discloses this particular feature. Brief at page 6.

Appeal No. 94-3053
Application 07/832,661

In response, the Examiner states on page 6 of the answer that:

[i]t would have been obvious to a person having ordinary skill in the art to provide a scan string selection logic network in accordance with the claims on the chip disclosed by Hester, because d'Angeac evidences the necessity of such logic.

However, a review of d'Angeac fails to reveal why a person of ordinary skill in the electronic processor art would have been motivated to modify Hester's support processor to include circuitry for selecting particular sensor circuits in the support processor. The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the

Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). We fail to find that the prior art suggests the circuitry for selecting as claimed

Appeal No. 94-3053
Application 07/832,661

by Appellants with the necessary reasons to combine it with the support processor of Hester. Therefore, we will not sustain this rejection.

Claim 3

Claim 3 stands rejected under 35 U.S.C. § 103 in view of Hester and Poret. On page 5 of the brief, Appellants set forth the only argument for this claim as follows: "[t]his rejection of Claim 3 is traversed for the same reasons given above (in Argument Section A) with respect to Claim 55."

Thus,

Appellants have not argued anything in addition to that which they argued for claim 55. Therefore, we will sustain the rejection of claim 3 for the reasons set forth above for claim 55.

This board declines to look beyond that which has been argued by Appellants. **Baxter**, 952 F.2d at 391, 21 USPQ2d at 1285; 37 CFR

§ 1.192.

Appeal No. 94-3053
Application 07/832,661

Claim 9

Claim 9 stands rejected under 35 U.S.C. § 103 in view of Hester, d'Angeac and Poret. Appellants argue that this rejection should be reversed because this claim recites that:

said serial scan circuit is interconnected with said counter for loading said counter with a value indicative of a predetermined count to which said condition sensor is thereby made sensitive,

and none of the references relied upon discloses these claimed features. Brief at 6.

In response, the Examiner states on page 8 of the answer that:

It would have been obvious to a person having ordinary skill in the art to provide Poret's on-chip counters in Hester's chip because they support the clearly desirable aspects of increased flexibility in controlling debugging operations.

However, a review of Poret and d'Angeac fails to reveal why a person of ordinary skill in the electronic processor art would have reason to modify Hester's circuitry to include Poret's counters such that the serial scan circuit would load

Appeal No. 94-3053
Application 07/832,661

the counters to a predetermined count for ultimately activating the condition sensor. We fail to find that the prior art suggests modifying Hester's serial scan circuit such that it is interconnected with said counter for loading said counter with a value indicative of a predetermined count to which said condition sensor is thereby made sensitive. Therefore, we will not sustain the Examiner's rejection of Appellants' claim 9.

Claim 10

Claim 10 stands rejected under 35 U.S.C. § 103 in view of Hester, d'Angeac and Poret. Appellants argue that this rejection should be reversed because this claim includes "a multiplexer having inputs connected to said sensor circuits and an output connected to said counter," and none of the references relied upon discloses these claimed features.

Brief at 6. In response, the Examiner states:

d'Angeac discloses testing a field replaceable unit, such as a chip, having plural scan strings (see column 1, lines 37-40). Each scan string **41**, including

Appeal No. 94-3053
Application 07/832,661

LSSD second latches serving as "condition sensors", is addressable by a on-chip addressing "logic network" **42-48** that provides a "multiplexer having inputs connected to said sensor circuits" for "determining selections of sensor circuits". LSSD latches **42-44** receive "control bits". It would have been obvious to a person having ordinary skill in the art to provide a scan string selection logic network in accordance with the claims on the chip disclosed by Hester, because d'Angeac evidences the necessity of such logic,

answer at 6, and

[a]s the examiner's answer indicates that d'Angeac provides scan loop string selection by a logic network 42-48 and the examiner's answer also indicates that Hester provides a counter in the form of a scannable control register IAR that can have its' data scanned out and in, no further response is deemed necessary,

supplemental answer at 2.

However, a review of the references relied upon fails to reveal why a person of ordinary skill in the electronic processor art would have any reason to modify Hester's circuitry to include "a multiplexer having inputs connected to said sensor circuits and an output connected to

Appeal No. 94-3053
Application 07/832,661

said counter." We fail to find a teaching of this limitation with the necessary suggestions found in the prior art to combine it with the circuitry of Hester. Therefore, we will not sustain the Examiner's rejection of Appellants' claim 10.

Claim 22

Claim 22 stands rejected under 35 U.S.C. § 103 in view of Hester. Appellants only argue that Hester fails to teach "said read-only memory is on-chip." Brief at 4. On this point, Hester discloses that:

The support processor may be a general purpose computer, such as an IBM PC, IBM Series 1, etc., containing programs which interface to the LSSD scan strings . . . to implement the required debug functions.

Col. 2, lines 51-55.

The above-described types of general purpose computers have read-only memory and, for saving space and cost reasons, such memory is typically on the same semiconductor chip as its related support processor or "condition sensor." To the extent that Hester's read-only memory may not have been

Appeal No. 94-3053
Application 07/832,661

on the same semiconductor chip as his support processor, it would have been obvious to a person of ordinary skill in the electronic processor art to put the memory and processor on the same chip in order to save space and the costs of an additional chip. **See *In re Sovish***, 769 F.2d 738, 743, 226 USPQ 771, 774 (Fed. Cir. 1985) (ordinary skill is presumed not something less). Accordingly, we will sustain the rejection of claim 22 under 35 U.S.C. § 103 in view of Hester.

Claim 27

Claim 27 stands rejected under 35 U.S.C. § 103 in view of Hester and d'Angeac. Appellants argue that this rejection should be reversed because this claim recites that:

said on-chip condition sensor includes . .
. a logic network connected to said sensor
circuits, said serial scan circuit being
. . . interconnected with said logic
network

for determining selections of sensor
circuits by said logic network,

Appeal No. 94-3053
Application 07/832,661

and neither Hester nor d'Angeac discloses these claimed features. Brief at 7.

In response, the Examiner states:

[i]t would have been obvious to a person having ordinary skill in the art to provide a scan string selection logic network in accordance with the claims on the chip disclosed by Hester, because d'Angeac evidences the necessity of such logic.

Answer at 6. However, a review of d'Angeac fails to reveal why a person of ordinary skill in the electronic processor art would have reason to modify Hester's support processor to include circuitry for selecting particular sensor circuits in the support processor. We fail to find a teaching of an on-chip condition sensor which includes a logic network connected to said sensor circuits, said serial scan circuit being interconnected with said logic network for determining selections of sensor circuits by said logic network with the necessary reasons found in the prior art to combine it with the support processor of Hester. Therefore, we will not sustain the Examiner's rejection of Appellants' claim 27.

Appeal No. 94-3053
Application 07/832,661

Claim 28

Claim 28 stands rejected under 35 U.S.C. § 103 in view of Hester and Poret. Appellants argue that this rejection should be reversed because this claim recites that:

said serial scan circuit being interconnected with said counter for loading said counter . . . with a value indicative of a predetermined count to which said condition sensor is thereby made sensitive,

and neither Hester nor Poret discloses these claimed features.

Brief at 4.

In response, the Examiner states:

It would have been obvious to a person having ordinary skill in the art to provide Poret's on-chip counters in Hester's chip because they support the clearly desirable aspects of increased flexibility in controlling debugging operations.

Answer at 8. However, a review of Poret fails to reveal why a person of ordinary skill in the electronic processor art would

have reason to modify Hester's circuitry to include Poret's counters such that the serial scan circuit would load the

Appeal No. 94-3053
Application 07/832,661

counters to a predetermined count for ultimately activating the condition sensor. We fail to find a teaching of a serial scan circuit being interconnected with said counter for loading said counter with a value indicative of a predetermined count to which said condition sensor is thereby made sensitive with the necessary reasons to modify the circuitry of Hester. Therefore, we will not sustain the Examiner's rejection of claim 28.

Claim 31

Claim 31 stands rejected under 35 U.S.C. § 103 in view of Hester and Poret. Appellants argue that this rejection should be reversed because this claim recites that:

counting occurrences of selected conditions of the electronic processor and producing a signal when a predetermined count is reached,

and neither Hester nor Poret discloses these claimed features.

Brief at 5. In response, the Examiner states:

Appeal No. 94-3053
Application 07/832,661

It would have been obvious to a person having ordinary skill in the art to provide Poret's on-chip counters in Hester's chip because they support the clearly desirable aspects of increased flexibility in controlling debugging operations.

Answer at 8. In view of the above discussion with regard to claim 28, we will not sustain this rejection.

Claim 61

Claim 61 stands rejected under 35 U.S.C. § 103 in view of Hester. Appellants concede that all of the limitations recited in that claim are met by Hester except:

issuing a signal from the on-chip condition sensor to the electronic processor upon detection of the predetermined condition.

Brief at 4-5.

However, Hester meets the above language by teaching that the support processor "include[s] the ability to examine and alter registers in the system microprocessor" (col. 2, lines 59-61) and "control[s] and examine[s] the contents of all

Appeal No. 94-3053
Application 07/832,661

facilities within the microprocessor [under test]" (col. 4, lines 6-7).

Hester performs this alter/control function by having a "desired instruction" that is used "to enable the stop-on-address function" of the microprocessor. Col. 3, lines 22-37; col. 4, line 10. Thus, the claim language that Appellants argue for claim 61 is met by Hester and since anticipation is the epitome of obviousness, **Fracalossi**, 681 F.2d at 794, 215 USPQ at 571, we will sustain the Examiner's rejection of claim 61 under 35 U.S.C. § 103 in view of Hester.

Aside from the above claim language for claim 61, Appellants have chosen not to argue any of the other specific limitations as a basis for patentability and this board declines to look beyond that which has been argued by Appellants. **Baxter**, 952 F.2d at 391, 21 USPQ2d at 1285; 37 CFR § 1.192.

Appeal No. 94-3053
Application 07/832,661

In view of the foregoing, the decision of the Examiner rejecting claims 2, 11-15, 17 and 55 under 35 U.S.C. § 102(b) and claims 3-5, 16, 20-26, 60 and 61 under 35 U.S.C. § 103 is affirmed; however, the decision of the Examiner rejecting claims 6-10, 27, 28 and 31 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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	Administrative Patent Judge)	
)	
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Appeal No. 94-3053
Application 07/832,661

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