

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today:  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

Paper No. 30

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS

MAILED

AND INTERFERENCES

APR 25 1996  
PAT. & T.M. OFFICE  
BOARD OF PATENT APPEALS  
AND INTERFERENCES

Ex parte TETSUYA MATSUMURA  
and MASAHIKO YOSHIMOTO

Appeal No. 94-2397  
Application 07/739,786<sup>1</sup>

HEARD: April 4, 1996

Before HAIRSTON, BARRETT and LEE, Administrative Patent Judges.  
LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of the appellant's claims 1-7 and 9-25, which are all claims remaining in the application.

The inventors will be collectively referred to as "appellant."

<sup>1</sup> Application for patent filed July 31, 1991. According to appellants, this application is a division of Application 07/489,946, filed March 9, 1990, now abandoned.

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References Relied on by the Examiner

Fujishima et al. (Fujishima)	4,586,167	April 29, 1986
Baumbaugh et al. (Baumbaugh)	4,809,232	February 28, 1989
Christopher	4,823,302	April 18, 1989
Matsumura et al. (Matsumura)	4,961,169	October 2, 1990

The Rejections on Appeal

Claims 1-7 and 9-25 were rejected under 35 U.S.C. § 112, first and second paragraphs because the examiner determined (Answer at 4) that (1) "the claimed invention is not described in such full, clear, concise and exact terms as to enable any person skilled in the art to make and use the same"; and that (2) the appellant failed "to particularly point out and distinctly claim the subject matter which applicant regards as the invention."

Claims 1-7, 9, 10 and 18-25 were rejected under 35 U.S.C. § 103 over the combined teachings of Christopher and Baumbaugh.

Claims 11-17 and 21 were rejected under 35 U.S.C. § 103 over Fujishima.

The Invention

The invention is directed to a serial memory access device such as that claimed in claim 21 and a specific application of a serial memory access device for progressive scan conversion of digital video data such as that claimed in claim 11. According to claim 21, the device comprises an array having a plurality of separately addressable cell areas, a plurality of access means

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each corresponding to a respective one of the cell areas, a plurality of activating means each corresponding to a respective one of the access means, a select signal storing means for generating a plurality of control signals, and selective coupling means responsive to the control signals for arranging the plurality of activating means in a predetermined circuit configuration.

Claim 21 reads as follows:

21. A serial access memory device, comprising:

a memory cell array having a plurality of separately accessible memory cell areas; each said area having memory cells disposed therein to store data signals;

a plurality of access means each respectively connected to a corresponding one of said plurality of memory cell areas for accessing memory cells in said corresponding one of said plurality of memory cell areas;

a plurality of activating means each respectively connected to a corresponding one of said plurality of access means and responsive to a clock signal for activating said corresponding one of said plurality of access means; and

select signal storing means for storing a selecting signal and generating a plurality of control signals determined by said selecting signal;

said activating means comprising selective coupling means responsive to said control signals generated by said select signal storing means for selectively coupling said plurality of activating means in predetermined circuit configurations.

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Claim 11 reads as follows:

11. A serial access memory device for converting first and second digital video data for progressive scan, comprising:

a memory cell array having four memory cell columns each having  $n$  memory cells disposed in  $k$  rows, where  $n$  and  $k$  are integers greater than one;

four writing means each respectively connected to a corresponding one of said four memory cell columns for writing one of the first or second video data in memory cells of said corresponding memory cell column;

first selecting means responsive to an externally applied first clock signal for alternately selecting a predetermined two of said four writing means;

said writing means selected by said first selecting means writing said first video data into memory cells of at least a first corresponding memory cell column;

second selecting means responsive to said externally applied first clock signal for alternately selecting the remaining two of said four writing means;

said writing means selected by said second selecting means writing said second video data into memory cells of at least a second corresponding memory cell column;

four reading means each respectively connected to a corresponding one of said four memory cell columns for reading stored data from memory cells therein; and

third selecting means responsive to an externally applied second clock signal for successively selecting individual ones of said four reading means,

said second clock signal having a frequency twice that of said first clock signal, and

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said reading means selected by said third selecting means respectively reading data stored in the memory cells of said memory cell column corresponding thereto.

Claim 11 requires that the reading clock signal frequency be twice that of the writing clock signal frequency. According to the specification, progressive scan conversion of video data results in time compressed video data such that the horizontal scanning lines in one field is doubled. (Spec. at 25-26)

OPINION

The claims have been properly grouped by the examiner. Merely arguing that the examiner has not addressed the limitations required by other independent or dependent claims does not satisfy the requirements set forth in 37 CFR § 1.192(c) (7) (iv).

However, proper grouping of claims by the examiner does not mean the examiner can simply not indicate which claim he is focusing on and deems as being representative of the group. It is still the claimed invention which must be examined, whichever claim of the group the examiner chooses to work with.

Because the appellant has not argued about not knowing which claim the examiner's reasonings were directed to, we will focus on claim 21 for the group containing claims 1-7, 9, 10, and 18-25, and claim 11 for the group containing claims 11-17 and 21.

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A. The rejection of claims 1-7,  
9, 10 and 18-25 over prior art

We reverse the rejection of claims 1-7, 9, 10 and 18-25 under 35 U.S.C. § 103 over the combined teachings of Christopher and Baumbaugh.

The examiner's stated reasons for this rejection are (Answer at 6):

Christopher shows a plurality of latches connected to parallel to serial interfaces. While Christopher does not specifically show a shift register connected thereto, from Baumbaugh et al. it would be obvious to one of ordinary skill in the art to use such in Christopher as a shift register is a convenient means of handling such serial data.

In his answer at 10, the examiner added:

As the examiner points out "a shift register is a convenient means of handling such serial data." Shift registers are an integral part of serial data manipulation and are routinely used, and well-understood in the art to be routinely used, whenever serial data is to be transferred to another processing section, the shift register acting as a buffer for the data. Buffers are so routinely used in the art for data handling that they are routinely left out to provide a more simplified picture of the disclosure. To use such a shift register in such an environment is wholly conventional and understood to one of ordinary skill in the art.

As shown in the above-quoted text, the examiner made some valid points. But those points are insufficient to support the rejection made. The claimed invention is not simply a shift register, a shift register generally employed as a buffer, or a shift register generally connected to latches. The fact that

shift registers were well known and commonly used for manipulating data does not establish that all inventions making use of shift registers for manipulation of data are unpatentable.

In the context of claim 21 and according to the appellant's disclosure, shift registers (Figure 6; Spec. at 12 and 19) implement the select signal storing means for storing a selecting signal and generating a plurality of control signals determined by said selecting signal. But claim 21 also recites the following elements none of which was accounted for by the examiner:

(1) a memory cell array having a plurality of separately accessible memory cell areas; each said area having memory cells disposed therein to store data signals;

(2) a plurality of access means respectively connected to corresponding memory cell areas for accessing data signals stored in memory cells of said respective memory cell areas;

(3) a plurality of activating means each connected to a corresponding one of said plurality of access means and responsive to a clock signal for activating said corresponding one of said plurality of access means; and

(4) said activating means comprising selective coupling means responsive to said control signals generated by said select signal storing means for selectively coupling said plurality of activating means in a predetermined circuit configurations.

The issue is not whether shift registers were well known, but why it would have been obvious to one with ordinary skill in the art to use all of the claimed elements, including a shift

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register as the select signal storing means, in the specific manner and configuration as has been set forth by the claims. As the appellant correctly argues (Br. at 17-18), the examiner failed to set forth any motivation for one with ordinary skill in the art to employ a combination of the elements claimed. The appellant also correctly argues (Br. at 17) that the examiner failed to address the other elements and relationships required by the claims.

We find that there was not any reasonably discernable attempt by the examiner to make the necessary underlying factual inquiries for determining obviousness as was prescribed by the Supreme Court in Graham v. John Deere Co., 383 U.S. 1, 17-18 (1966). Specifically, the scope and content of the prior art must be determined. The differences between the claimed invention and the prior art must be ascertained. The level of ordinary skill in the art must be assessed. And any objective evidence of nonobviousness must be considered. Here, if the examiner has made the necessary inquiries, the factual determinations have not been sufficiently articulated or otherwise made known. In summary, the rejection has not been sufficiently developed or explained to permit meaningful review.

What are the plurality of access means in Christopher, each of which being respectively connected to a corresponding one of a plurality of memory cell areas for accessing data from cells in

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that area? What are the plurality of activating means in Christopher, which respectively activates a corresponding one of the access means? What are the multiple selective coupling means in Christopher, which couple selected ones of the activating means in a predetermined circuit configuration? Where in Christopher are two activating means coupled to form a predetermined configuration in response to control signals generated by a select signal storing means? Why would those elements be suggested by the combined teachings of Christopher and Baumbaugh? Those questions have to be accounted for in a proper rejection.

We will not speculate as to what the examiner had in mind when comparing the cited references with the appellant's claimed invention. It is also not the role of the Board to perform examination in the first instance. For the foregoing reasons, because the examiner failed to establish a prima facie case of obviousness, the rejection of claims 1-7, 9, 10, and 18-25 is reversed.

The rejection of claims  
11-17 and 21 over Fujishima

We reverse the rejection of claims 11-17 and 21 under 35 U.S.C. § 103 over Fujishima.

In support of rejecting claim 11 over Fujishima, the examiner indicates (Answer at 6): (1) Fujishima discloses a

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"nibble" shift register; (2) clocking the shift register by a two-phase clock would have been obvious; (3) using the so clocked shift register in a video environment to process video signals would have been obvious; and (4) using any size memory cell array would have been obvious to one with ordinary skill in the art. In his answer at 9, the examiner added that the video aspects of the claimed invention reflects just a statement of intended use, that two-phase clocking was notoriously well known, and that a four bit "nibble" signal can be used in many applications.

Claim 11, however, does not claim just a "nibble" shift register, a "nibble" shift register generally used for video applications in the abstract, or a "nibble" shift register timed by a two-phase clock. Instead, claim 11 sets forth a collection of specific elements which interact in a specific manner to convert first and second digital video data for progressive scan. The specificity with respect to which video data and video signals are intertwined with the claimed structural components and functional cooperation therebetween exceeds that which can reasonably be deemed as merely an intended use recitation.

Claim 11 defines a memory cell array having four columns, four writing means each associated with a respective corresponding one of the four memory cell columns, four reading means each associated with a respective corresponding one of the four cell memory columns, a first clock signal, a second clock

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signal having twice the frequency of that of the first clock signal, a first selecting means responsive to the first clock signal for "alternately" selecting a predetermined two of the four writing means, a second selecting means responsive to the first clock signal for selecting the remaining two writing means, and third selecting means responsive to the second clock signal for selecting individual ones of the four reading means. The apparatus so claimed permits conversion of first and second digital video data for progressive scan.

The appellant argues (Br. at 14) that while Fujishima discloses nibble mode memory access, that is unrelated to the subject matter of the claims and there is no motivation to make modifications to Fujishima which are necessary to result in the combination of elements required by the claimed invention.

The examiner failed to explain or otherwise demonstrate how Fujishima's disclosure satisfies or would render obvious the structural elements and functional interactions required by appellant's claim 11. Where in Fujishima is a first selecting means, responsive to a clock signal, which "alternately" selects two of four writing means each associated with a corresponding column of the memory array? Where in Fujishima is a second selecting means which selects the remaining two of the four writing means responsive to the same clock signal? Where in Fujishima is a third selecting means responsive to a second clock

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signal having a frequency twice that of the first clock signal for selecting individual ones of the four reading means?

As has already been noted above, the obviousness question under 35 U.S.C. § 103 requires the examiner to make underlying factual findings on the scope and content of the prior art and differences between the claimed invention and the prior art. Whatever the examiner had in mind when he studied Fujishima and when he compared the claimed invention with Fujishima's disclosure, he did not express it in sufficient detail to enable meaningful review. For instance, if the examiner thought "nibble" mode access of memory via a shift register satisfies the claimed invention, he has not explained how. On this record, the lack of adequate and pertinent findings by the examiner indicates that the necessary Graham v. John Deere underlying factual inquiries were not made. The rejection was improper.

We will not speculate as to what the examiner had in mind but failed to make known in his rejection of the claims. It is also not the role of the Board to engage in substantive examination in the first instance. Accordingly, because the examiner failed to set forth a prima facie case of obviousness, the rejection of claims 11-17 and 21 is reversed.<sup>2</sup>

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<sup>2</sup> Even if we selected claim 21 to focus on, the result would be the same for essentially the same reasons, i.e., the examiner made insufficient factual findings about the scope and content of the prior art and differences between the claimed invention and the

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The rejection of claims 1-7 and 9-25 under  
35 U.S.C. § 112, first and second paragraphs

We reverse the rejection of claims 1-7 and 9-25 under  
35 U.S.C. § 112, first and second paragraphs.

As is the case with the rejections based on prior art, the  
rejection for lack of enabling disclosure under 35 U.S.C. § 112,  
first paragraph, is based on inadequate findings and insufficient  
explanation. As to claim 1, the examiner states (Answer at 4):

Claim 1 recites "select signal storing means for  
storing a selecting signal," but there is apparently a  
lack of supporting disclosure which would enable anyone  
skilled in the art to be able to make and use the same.

What is the basis for concluding that the disclosure would  
not have enabled one with ordinary skill in the art to construct  
a select signal storing means for storing a selecting signal? No  
explanation was offered by the examiner, except that he further  
stated (Answer at 4):

Whether there is adequate support in the specification  
or not is thus not a matter of reasoned inquiry but  
rather one of wild conjecture.

If the determination of lack of enablement is based on the  
examiner's "wild conjecture," as the examiner himself has so  
characterized his conclusion, the rejection cannot be sustained.  
If the rejection is based on well founded factual findings and  
logical reasoning, such has not been articulated or otherwise

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prior art to support a prima facie case.

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made known, and so the rejection also cannot be sustained.

In any event, the appellant properly points out (Br. at 3) that the specification at 11-12 describes the select signal storing means and that Figure 6 specifically illustrates the select signal storing means (Br. at 8). We note further that operation of the select signal storing means as illustrated in Figure 6 is particularly described in the specification at 19-20. The examiner has failed to explain why such abundance of description is inadequate to enable one with ordinary skill in the art to make and use a select signal storing means as claimed. Is it because the specification does not state that a separate select signal for each programmable flip flop would be outputted by the select signal storing means shown in Figure 6? The examiner has not said. If it is, the examiner has not explained why one with ordinary skill in the art would not have known how to use the select signal storing means shown in Figure 6 to output a different select signal for each programmable flip flop without undue experimentation. Without specific findings and a reasoned rationale, not only is the rejection essentially unreviewable, the appellant was also left without a fair opportunity to respond to the rejection.

The appellant should not have to and we decline to speculate on what the examiner had in mind when the rejection was made. The specification further describes at 31 to 32 that a ROM may be

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used as the serial interface circuit. The examiner indicates (Answer at 7) that how the shift register shown in Figure 6 relates to the referenced ROM is not clear. But the ROM is simply an alternative implementation of the select signal storing means with respect to the shift register. Even if the shift register implementation is assumed to be unenabling, why would the ROM implementation be unenabling insofar as the need to output a series of control signals S1 - S10 for each programmable flip flop is concerned? The examiner has not explained

The examiner stated (Answer at 4-5):

It is not clear that there is adequate supporting disclosure for "a plurality of writing/reading means each connected to one of said plurality of memory cell columns," etc. . . .

It is not clear that there is adequate supporting disclosure for "m writing means each respectively connected to a corresponding one of said m memory cell columns."

Again, what the examiner had in mind is not known. What did the examiner think of the plurality of bit line drivers DI shown in Figure 7 each for writing data into a corresponding memory column? What did the examiner think of the plurality of sense amplifiers DO shown in Figure 7 each for reading data from a corresponding memory column? There is particular description in the specification at 20 for such bit line drivers for writing and sense amplifiers for reading. What did the examiner think of those portions of the specification? We decline to guess.

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As to the vague and indefiniteness rejection under 35 U.S.C. § 112, second paragraph, there is likewise an inadequate explanation. And to the extent the examiner has explained, we find his position to be erroneous.

The examiner stated (Answer at 4):

The elements 23 corresponding to 14 are first described as "selecting means," then "enabling means," then "activating means." The claims are filled with such meaningless designators.

Why are the various functional means recited in the claims regarded as "meaningless designators"? We will not speculate. It is incumbent on the examiner to explain his position.

In any event, we disagree that the functional means recited in the claims are meaningless designators. To begin with, 35 U.S.C. § 112, sixth paragraph, expressly authorizes a patent applicant to use such means-plus-function language. In particular, 35 U.S.C. § 112, sixth paragraph states:

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

In In re Donaldson Co., Inc., 16 F.3d 1189, 1192-1195, 29 USPQ2d 1845, 1848-1850 (Fed. Cir. 1994) (in banc), the Federal Circuit expressly held that 35 U.S.C. § 112, sixth paragraph, applies during patent examination as well as in post-issuance situations.

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As is recited in claim 21, each activating means is respectively connected to a corresponding one of the plurality of memory access means and is responsive to a clock signal for activating the corresponding access means. As is shown in Figure 3 and described in the specification at 13, each activating means is a programmable flip flop 23 which outputs an enable signal "for enabling or activating the bit line driving circuit 18 or the sense amplifier circuit 19 for one column." That the specification also uses the term "enabling" when describing "activating" does not make the claimed activating means indefinite. Indeed, it is an "enable signal" that is outputted by the activating means.

Contrary to the examiner's suggestion, we can find no recitation in the claims to an "enabling means." As to the selecting means, claim 11 recites that it is responsive to externally applied control signals for selecting various ones of the plurality of reading and writing means. As disclosed in the specification, the selecting means is the specific arrangement of interconnected flip flops 23 the coupling of which to each other is made in accordance with the control signals outputted from the select signal storing means or serial interface circuit 22. We find nothing indefinite about appellant's use of means language.

The examiner further stated (Answer at 5) that appellant's references to "NTSC video data" and "NTSC standard video signals"

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are vague and indefinite. We disagree. The fact that the terms cover every video standard of NTSC for video data and video signals means the terms are broad. Also, if some formats conform to NTSC standards as well as PAL or SECAM standards, it is nonetheless within the scope of the claims requiring the data or signals to conform to NTSC standards. The examiner confused breadth of claim scope with indefiniteness. The examiner's contention that NTSC signals are analog while the claimed invention is digital is misplaced. As the appellant has pointed out (Reply at 7), digital processing of video signals is well known. The claims reciting NTSC video data and signals simply limit the digital processing to data and signals conforming to NTSC standards.

Claims 3, 12 and 18-19 evidently require a ring pointer structure. The examiner first contended (Answer at 5) that the term "ring pointer" does not appear to be well defined. But thereafter, the examiner stated (Answer at 8):

That the term "ring pointer" may be a term of art is not in question. What is in question is whether appellants actually have such disclosed with sufficient particularity as to be enabling to anyone skilled in the art. The examiner has concluded that there is not, at least in the present environment and urges the Board to hold likewise.

The above-quoted text fittingly illustrates the deficiency in the examiner's position. The examiner concluded that there was no enabling disclosure for a ring pointer, but offered no

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reasoning.

We agree with the appellant (Br. at 12) that in the context of the specification, a "ring pointer" is a structure which outputs a series of distinct signals in a circulating fashion. The appellant's disclosed flip flops 23, programmably configurable to form looped structures shown in Figure 3 and 9 indeed constitute "ring pointers" as are described in the specification at 13, 17-18 and 28. The examiner nowhere explained why they do not, or why it would require undue experimentation for one with ordinary skill in the art to construct the programmable flip flops specifically shown in appellant's Figures 4A and 4B and correspondingly described in the specification at 12 and 14 and then to connect them in a cascaded manner to form a ring pointer.

The appellant cited to Matsumura to show that the term "ring pointer" is not an indefinite term but was known and has been used in the art. But that does not mean the appellant's specifically disclosed ring pointer structure has to be the same as the one disclosed in Matsumura in order to have meaning. The appellant's ring pointer is formed of programmably configurable and cascadably connectable flip flops, which is simply different from that disclosed in Matsumura. Accordingly, the examiner's effort to find specific correspondence between Matsumura's ring pointer and the appellant's disclosed ring pointer is misplaced.

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The appellant does not dispute that the specific ring pointer structure disclosed in the specification and that disclosed in Matsumura are different (Br. at 12-13). In any event, as has been pointed out by the appellant (Reply at 4), the ring pointer structure in Matsumura is also looped as is the case with the appellant's disclosed ring pointer. See Matsumura at column 5, lines 47-51. In that regard, we see no inconsistency in the appellant's use of the term "ring pointer."

Finally, with respect to claim 14, the examiner stated (Answer at 5):

It is not clear that there are adequately disclosed and supported "first and second serial data" supplies, as is claimed in claim 14.

Again, the examiner merely concluded without making underlying factual findings and/or pertinent explanations. What effort did the examiner make to determine that there is no adequate disclosure for the feature referred to? What basis and which facts caused the examiner to come to his conclusions? It is also uncertain whether the examiner was referring to the written description requirement or the enablement requirement of 35 U.S.C. § 112, first paragraph, which are distinctly different from each other. With respect to all of these uncertainties, we decline to speculate as to what the examiner had in mind and reiterate that it is not the role of the Board to conduct patent examination in the first instance.

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The proposed drawing correction that was refused entry by the examiner

The appellant raises for our consideration the issue whether the drawing changes submitted on February 12, 1991, constitute new matter as has been determined by the examiner (Br. at 7 and 13-14). The appellant explains (Reply at 9) that it is not seeking review by the Board of the petitionable question whether the examiner's refusal of entry of the drawing amendment<sup>3</sup> was proper, but simply the examiner's determination that the proposed drawing change adds new matter to the original specification.

The appellant further asserts (Reply at 9) that the examiner placed the new matter issue before the Board by making a Final Rejection based on new matter and has repeated in his answer the rejection based on new matter. Even if the appellant is correct, that does not mean the issue has to be addressed. We decline to address it because it is mooted by our reversal of the rejection made under 35 U.S.C. § 112, first paragraph. The examiner is correct that we need only determine whether the specification as originally filed supports the subject matter of the claims. And we did.

Since no rejection of the claims remains outstanding, the examiner's characterization of the proposed drawing change as

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<sup>3</sup> The examiner's answer indicates that the proposed drawing change was not entered.

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adding new matter and consequent refusal to enter the drawing change need not be reviewed by the Board.

Conclusion

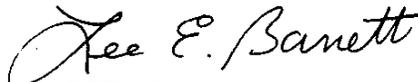
The rejection of claims 1-7 and 9-25 under 35 U.S.C. § 112, first and second paragraphs, is reversed.

The rejection of claims 11-17 and 21 as being unpatentable under 35 U.S.C. § 103 over Fujishima is reversed.

The rejection of claims 1-7, 9, 10 and 18-25 as being unpatentable over Christopher and Baumbaugh is reversed.

REVERSED

  
KENNETH W. HAIRSTON  
Administrative Patent Judge )

  
LEE E. BARRETT  
Administrative Patent Judge )

  
JAMESON LEE  
Administrative Patent Judge )

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