Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte SHIGERU KURODA, YASUTOSHI OKUNO and KEN NUMATA

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Appeal No. 2003-2096
Application No. 09/847,202

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ON BRIEF

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Before GARRIS, WALTZ, and DELMENDO, **Administrative Patent Judges.**

WALTZ, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on an appeal from the primary examiner's final rejection of claims 2 and 4 through 7, which are the only claims remaining in this application. We have jurisdiction pursuant to 35 U.S.C. § 134.

According to appellants, the invention is directed to an integrated circuit structure comprising a semiconductor material having active regions with a gate structure thereon, with an isolation region in the semiconductor material having a trench

and electrically insulating liner (Brief, page 2). A first portion of the isolation region extends to the surface of the semiconductor material, a second portion of the isolation region extends above and within the confines of the trench, and a dielectric sidewall spacer is disposed on and extends over the isolation region (*id.*).

Appellants state that the claims do not stand or fall together (Brief, page 3) and present reasonably specific reasons for the separate patentability of each claim (Brief, page 5). Accordingly, to the extent appellants have separately argued the dependent claims, we consider each claim separately. See 37 CFR § 1.192(c)(7)(2000). A copy of independent claim 4 as found in this application is attached as an Appendix to this decision.

In addition to appellants' admitted prior art (see Figures 3-6d), the examiner relies on Luning, U.S. Patent No. 6,005,279, issued on Dec. 21, 1999 (filed Dec. 18, 1997), as evidence of obviousness. The claims on appeal stand rejected under 35 U.S.C. § 103(a) as unpatentable over the admitted prior art (Figures 3-6d) in view of Luning (Answer, page 3). We *affirm* the rejection on appeal essentially for the reasons set forth in the Answer and those reasons stated below.

OPINION

The examiner finds that appellants' prior art figures show an integrated circuit structure comprising active regions of semiconductor material (660), an isolation region (610) within a trench of the semiconductor material, an electrically insulating liner (620) disposed in the trench with a portion of the liner extending over the active region, a first portion of the isolation region conformal to the surface of the semiconductor material, and a second portion of the isolation region extending above the surface of the active regions (Answer, pages 3-4). The examiner finds that the prior art figures 3-6d show all the claimed elements except the sidewall spacers on the isolation region (Answer, page 4).

The examiner applies Luning to show a trench isolation structure in which dielectric sidewall spacers (52) are formed on and extending over an isolation region (47) and inclined toward the isolation region from a semiconductor surface (41) to prevent oxide loss at the edge of the trench during etching (*id.*). From these findings, the examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the isolation structure of prior art figures 3-6d by adding dielectric sidewall spacers as taught by Luning to prevent oxide loss at the edge of the trench during subsequent etching steps (*id.*). We agree.

Appellants argue that the claimed provision of providing a dielectric sidewall spacer on and extending over the isolation region extending above the active regions is not taught or suggested by the combination of admitted prior art and Luning, even assuming arguendo that the combination is proper (Brief, page 4). Appellants further argue that the spacer 52 in Luning is not disposed over the isolation region as required by the claims on appeal, the insulating material 47 of Luning is not partially conformal with the surface of the semiconductor material and partially extending over that surface, the liner 46 of Luning does not extend out of the isolation region and over the active region, and there is no suggestion to install the features of Luning into the admitted prior art (Brief, page 4).

Appellants' arguments are not persuasive. As admitted by appellants, all the claimed features are shown by the admitted prior art figures with the exception of the dielectric sidewall

spacers (Answer, page 5, citing the Brief, page 4, ll. 4-5). Therefore appellants' arguments that Luning fails to disclose the claimed location of the insulating material and liner are not well taken as these features and their locations were shown in the admitted prior art (Figures 3-6d). As correctly stated by the examiner (Answer, paragraph bridging pages 5-6), Luning discloses an inclined sidewall spacer 52 disposed "on and extending over said isolation region" as required by claim 4 on appeal since the isolation region includes the trench (45), the liner (46), and the insulation/central portion (47). Accordingly, appellants' argument that the spacer 52 of Luning is not disposed over the isolation region as required by the claim is not persuasive. Finally, appellants' argument that there is no suggestion to install the features of Luning into the admitted prior art is not persuasive for the reason noted by the examiner, namely that the motivation for using the sidewall spacers of Luning in the structure of the admitted prior art is "to prevent oxide loss at the edge of the trench during an etching step" (Answer, page 4). As noted by appellants, in the prior art there was a problem with penetration into the shallow trench isolation

(STI) after a contact etch (specification, page 4, ll. 5-15). This same problem was recognized by Luning, i.e., oxide loss at the edges of isolation trenches during subsequent etching (col. 2, ll. 58-61; col. 4, ll. 1-7; ll. 42-59; col. 6, ll. 21-25; and col. 7, ll. 47-51), and was solved by the installation of sidewall spacers.

Appellants argue that though Luning teaches the use of a sidewall, that sidewall is placed at a location different from that of the invention (Reply Brief, pages 2-3). This argument is not persuasive since, as correctly found by the examiner, Luning teaches that the sidewall 52 is placed at a location corresponding to the location required by claim 4 on appeal, i.e., on and extending over the isolation region, inclined toward the isolation region and over a portion of the liner. The placement of the sidewall spacer "at the shoulder" (Reply Brief, page 2) is not recited in the claims on appeal.

With regard to appellants' arguments concerning claims 2 and 5-7, we adopt the examiner's findings from page 6 of the Answer, namely that Luning discloses the claim 5 limitation that the sidewall spacer is made from silicon nitride or silicon oxide

(see col. 4, ll. 48-50) while the claim 6 and 7 limitations have been taught by the admitted prior art figures. With regard to the claim 2 limitation, the examiner notes that figure 5 of Luning shows that no portion of the sidewall spacers 52 lie on top of the second portion of the isolation region (Answer, page 6).

For the foregoing reasons and those stated in the Answer, we determine that the examiner has established a *prima facie* case of obviousness based on the reference evidence. Based on the totality of the record, including due consideration of appellants' arguments, we determine that the preponderance of the evidence weighs most heavily in favor of obviousness within the meaning of section 103(a). Accordingly, the rejection of the claims on appeal under section 103(a) over the admitted prior art in view of Luning is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

BRADLEY R. GARRIS Administrative Patent Judge	)	
THOMAS A. WALTZ Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ROMULO H. DELMENDO Administrative Patent Judge	)	

TAW/vsh

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APPENDX

4. An integrated circuit structure, comprising:

semiconductor material having, active regions with a gate structure thereon;

an isolation region comprising a trench in said semiconductor material having an electrically insulating liner on the surface of said trench, a first portion of said isolation region extending to the surface of said semiconductor material and conformal to said semiconductor surface, a second portion of said isolation region extending above and within the confines of said trench, said second portion extending above the surface of said active regions of semiconductor material and separating said active regions of semiconductor material, said liner extending over said active region; and

a dielectric sidewall spacer on and extending over said isolation region extending above said active regions of said semiconductor material and inclined toward said isolation region from said semiconductor surface and over a portion of said liner extending over said active region.