

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HARIKLIA DELIGIANNI, JOHN OWEN DUKOVIC, DANIEL CHARLES EDELSTEIN, WILMA JEAN HORKANS, CHAO-KUN HU, JEFFREY LOUIS HURD, KENNETH PARKER RODBELL, CYPRIAN EMEKA UZOH and KWONG-HON WONG

Appeal No. 2003-0623
Application No. 09/348,632

HEARD: June 11, 2003

Before PAK, OWENS, and POTEATE, Administrative Patent Judges.
CHUNG K. PAK, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1 through 6, 8, 9, 11 through 25, 40 through 50 and 109 through 123. Claims 26 through 39 and 51 through 108, the remaining claims in the above-identified application, have been withdrawn from consideration by the examiner as being drawn to a non-elected invention.

Claims 1 and 115 are representative of the subject matter on appeal and read as follows:

1. A process for fabricating an interconnect structure on an electronic device with void-free seamless submicron conductors comprising the steps of:

forming an insulating material on a substrate,

lithographically defining and forming recesses for submicron lines and/or submicron vias in said insulating material in which interconnection conductor material will be deposited,

forming a conductive layer on said insulating material serving as a plating base,

depositing by a damascene process said conductor material in a seamless and void-free manner by electroplating from a bath containing additives, said bath additives causing the plating rate to increase with depth along the sidewall of a recess, thereby preventing the formation of a seam or void in a conductor in said recesses, and said conductor material comprising copper and

planarizing the resulting structure to accomplish electrical isolation of individual seamless and void-free lines and/or seamless and void-free vias.

115. The process of claim 2 wherein the copper is deposited in a double damascene structure.

The prior art references relied upon by the examiner are:

Aigo	4,339,319	Jul. 13, 1982
Poris	5,256,274	Oct. 26, 1993
Chang et al. (Chang)	5,266,446	Nov. 30, 1993
Gelatos et al. (Gelatos)	5,391,517	Feb. 21, 1995
Jain	5,602,423	Feb. 11, 1997
Huang et al. (Huang)	5,635,423	Jun. 3, 1997

Lowenheim, *Electroplating*, McGraw-Hill Book Co., pp. 198-202 (1978).

Silman et al. (Silman), *Protective and Decorative Coating for Metals*, Finishing Publications LTD., pp. 310-314 (1978).

The references relied upon by the appellants are:

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Li et al. (Li), "Copper-Based Metallization in ULSI Structures," *MRS Bulletin*, pp. 15-18 (August 1994).

Andricacos et al. (Andricacos (I)), "Damascene Copper Electroplating for Chip Interconnections," *IBM J. Rec. Develop.*, Vol. 42, No. 5, pp.567-573 (September 1998).

Andricacos (Andricacos (II)), "Copper On-Chip Interconnections: A Breakthrough in Electrodeposition to Make Better Chips," *Interface*, The Electrochemical Society, Inc., Vol. 8, No. 1, pp. 32-37 (Spring 1999).

Bulkeley (Bulkeley (I)), "The first copper-based ICS debut," *Design News Semiconductors*, pp. S11-S14 (June 7, 1999).

Alterio, "IBM Deal Features New Chip: Power4 Will Drive a New German Supercomputer," *The Journal News*, (Unknown Publication Date).

Bulkeley (Bulkeley (II)), "IBM, Sony Set Game Plan for PlayStation 3 Chips," *ZDNet News* (Unknown Publication Date).

The appealed claims stand rejected as follows:

- 1) Claim 116 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention;
- 2) Claim 116 under 35 U.S.C. § 112, first paragraph, as lacking written descriptive support for the subject matter presently claimed;
- 3) Claims 1 through 6, 8, 9, 11, 110, 111, 113 through 115, and 117 through 123 under 35 U.S.C. § 102(b) as anticipated by Chang alone or Chang as interpreted in view of Poris and Silman;

- 4) Claims 1 through 6, 8, 9, 11, 110, 111, 113 through 115 and 117 through 123 under 35 U.S.C. § 103 as unpatentable over the combined disclosures of Chang, Poris and Silman.
- 5) Claims 15 through 25, 40 through 50, 112 and 116 under 35 U.S.C. § 103 as unpatentable over the combined disclosures of Chang, the admitted prior art and Lowenheim;
- 6) Claims 12 through 14 under 35 U.S.C. § 103 as unpatentable over the combined disclosures of Chang, the admitted prior art, Lowenheim and Aigo;
- 7) Claims 1 through 6, 8, 9, 11, 15 through 25, 40 through 50 and 109 through 123 under 35 U.S.C. § 103 as unpatentable over either Jain, Gelatos or Huang, and Poris and the admitted prior art; and
- 8) Claims 12 through 14 under 35 U.S.C. § 103 as unpatentable over either Jain, Gelatos, or Huang, and Poris, the admitted prior art and Aigo.

We reverse each of the foregoing rejections.

We reverse the examiner's Section 112 rejections for essentially those reasons set forth at pages 5 and 6 of the Brief. Notwithstanding the examiner's arguments to the contrary, we concur with the appellants that one of ordinary skill in the art would have appreciated that at least some of the additives specifically mentioned in the specification are polarizing materials. See attached Grant & Hackh's Chemical Dictionary, Fifth Edition, pages 459-460 (1987). Not only is the term "polarizing" clear to those of ordinary skill in the art, but it also is inherently or implicitly described

in the specification as originally filed. Id. It then follows that the use of the terminology “polarizing” in the appealed claims does not violate the requirements of the first and second paragraphs of 35 U.S.C. § 112.

We also reverse the examiner Sections 102 and 103 rejections for essentially those reasons set forth at pages 6 through 24 of the Brief. We only add that the examiner, on this record, has not demonstrated that the deposition methods disclosed in the applied prior art references are useful for depositing a particular conductive material in recesses for **submicron lines or submicron vias** to advantageously obtain an interconnect structure on an electronic device with **void-free seamless submicron conductors**. This is especially true in this case since Poris, one of the prior art references relied upon by the examiner, teaches away from using the claimed deposition method to form void-free seamless submicron conductors as indicated by the appellants. See also, Poris, Figure 1A, together with Poris, column 4, lines 49-62. It then follows that one of ordinary skill in the art would not have readily envisaged, or would not have been led to use, the claimed deposition method (inclusive of, e.g., the types of the electroplating bath compositions and conditions capable of providing **void-free seamless submicron conductors not recognized by the applied prior art references**) to form the claimed interconnect structure on an electronic device within the meaning of 35 U.S.C. §§ 102 and 103.

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In view of the foregoing, the decision of the examiner is reversed.

REVERSED

CHUNG K. PAK)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
TERRY J. OWENS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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LINDA R. POTEATE)	
Administrative Patent Judge)	

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