

The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EDWARD BRIAN BOLES, RODNEY JAY DRAKE,
DARREL RAY JOHANSEN, SUMIT K. MITRA,
JOSEPH TRIECE and RANDY YACH

Appeal No. 2003-0194
Application No. 09/280,112

HEARD: AUGUST 19, 2003

Before KRASS, JERRY SMITH and RUGGIERO, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-142.

The invention is directed to a microprocessor using a memory bank system. The inventive system includes a data memory divided into n banks and a bank select unit. A memory bank system is

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used whenever a CPU is not able to address the whole linear address space. A memory bank select unit uses a special function register which selects one of the memory banks. The selected bank is then coupled with the CPU. The CPU cannot address any other banks while processing standard instructions. All standard instructions are then limited to the selected memory bank. To access different locations within the memory, a different memory bank has to be selected by the bank select unit.

Representative independent claim 2 is reproduced as follows:

2. A microcontroller comprising:

a central processing unit;

a data memory coupled with said central processing unit being divided into n banks;

said central processing unit comprising:

-a bank select unit for selecting one of said banks in said data memory, wherein said selected bank forms a register file;

-an arithmetic logic unit coupled with said register file;

-a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit.

The examiner relies on the following references:

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Noguchi et al. (Noguchi)	5,117,488	May 26, 1992
Lau et al. (Lau)	5,553,023	Sep. 03, 1996

Claims 1-142 stand rejected under 35 U.S.C. § 103 as unpatentable over Noguchi in view of Lau.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teachings, suggestions or implications in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051,

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5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc. , 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See Id.; In re Hedges, 783 F.2d 1038, 1040, 228 USPQ 685, 687 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 146-47 (CCPA 1976). Only those arguments actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief have not been considered and are deemed to be waived (see 37 CFR 1.192 (a)).

The examiner applies Noguchi for allegedly teaching a data processing system comprising a CPU, a linearized address space

and a working register within the CPU "mapped in the data memory" (answer-page 3). The examiner asserts that Noguchi "did not expressly detail" that the microcontroller was capable of any operations on any register in any addressing mode; that a program counter was used; and that there is a means and method for selecting between a memory and a virtual bank wherein the virtual bank comprised a combination of a partial memory space of the two memory banks.

With regard to the first two denoted differences, the examiner merely asserted the obviousness of not restricting matching any of the addressing modes with any of the instruction operations and of a program counter for keeping track of the current instruction being executed.

With regard to the selecting between a memory and a virtual bank, the examiner cites Lau for a virtual memory bank "where boundaries for the virtual banks were designated to be with two different memory banks" (answer-page 4) and finds that it would have been obvious that "the bits used to indicate whether the virtual bank boundary was enabled and the memory mapping means (e.g., see fig.2) would have comprised means to select a virtual or non-virtual memory bank in the Lau system" (answer-page 4).

The examiner also asserts that it would have been obvious to

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combine the teachings of Noguchi and Lau because Noguchi "used orthogonal instruction sets and therefore would have the need to separate the data in processing one instruction set with another instruction set. In the partitioning memory space is lost. Lau provided a method for recovering the lost memory space by providing virtual memory banks. These virtual memory banks clearly would have provided increased efficiency to the Noguchi system..." (answer-page 4).

We find that the examiner has not set forth a prima facie case of obviousness with regard to the claimed subject matter. Accordingly, we will not sustain the examiner's rejection of claims 1-142 under 35 U.S.C. § 103.

First, even if Noguchi and Lau disclosed everything they are alleged to disclose, which they do not, there would have been no reason to combine these references. Noguchi has nothing whatsoever to do with dividing memory into n banks, with a bank select unit for accessing one of the banks or a virtual bank. Therefore, to the extent that Lau might teach a bank select unit, as claimed, there would have been no reason other than impermissible hindsight for modifying anything in Noguchi with Lau's teachings.

Moreover, we find nothing in either of the applied

references, nor has the examiner convincingly pointed to anything in these references, showing a bank select unit for selecting a bank wherein the selected bank "forms a register file" (as in instant claim 2). Since there is no register file, there can be no "arithmetic logic unit coupled with said register file." Further, the mapping described in Lau (where a memory controller "maps" all of the memory locations in a virtual memory bank to a first area on a memory map) does not appear to be the mapping claimed, i.e., "a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit" (claim 2).

With regard to the "working register," the examiner relies on element 401 of Noguchi. We do not regard this element as a "working register," as set forth in instant claims 1 and 2, because no "special function" (claim 2) or mapping of this "working register" in a data memory (claim 1) has been shown by the examiner. To the extent the examiner relies on Lau, as explained supra, there would have been no reason to modify any register in Noguchi in order to arrive at the claimed "working register."

With regard to the claimed "bank select unit," the examiner

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appears to rely on Lau, but Lau discloses, not a bank select unit," as claimed, but a memory controller which, in conjunction with other elements, is used to allow mapping of a portion of a memory unit to fill holes in the logic memory which are smaller than the physical capacity of the memory unit. Lau does not appear to "select" a memory bank, as required by the instant claims and, since Noguchi clearly does not perform this function either, the examiner's rejection is not convincing as to an important claim limitation.

The examiner's decision rejecting claims 1-142 under 35 U.S.C. § 103 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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JERRY SMITH)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
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JOSEPH F. RUGGIERO)	
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