

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 38

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte EDGAR HOLMANN  
and TOYOHICO YOSHIDA

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Appeal No. 2002-2330  
Application No. 09/116,260

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ON BRIEF

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Before BARRETT, BARRY, and LEVY, Administrative Patent Judges.  
LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 36, 37 and 39-42. Claims 13, 15-17, 19, 21 and 22 have been allowed by the examiner. Claim 38 has been objected to.

BACKGROUND

Appellants' invention relates to a microprocessor having delayed instructions. An understanding of the invention can be

derived from a reading of exemplary claim 36, which is reproduced as follows:

36. A microprocessor comprising:

an instruction decoder receiving a delayed instruction from a memory, for decoding the delayed instruction to output a control signal, said delayed instruction including a field for specifying a delay value;

a program counter for calculating and outputting an address value designating a location of the memory at which an instruction to be processed is stored to control a program sequence; and

an instruction execution unit performing an operation specified by the delayed instruction based on the control signal in a case of a coincidence between a value of said program counter and a first program counter value which is specified by the field of the delayed instruction as the delay value.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Morrison et al. (Morrison)	4,847,755	Jul. 11, 1989
Hagqvist et al. (Hagqvist)	5,581,776	Dec. 3, 1996

Claims 36, 37 and 39-42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagqvist in view of Morrison. Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejection, we make reference to the examiner's answer (Paper No. 36, mailed May 20, 2002) for the examiner's complete reasoning in support of the

rejection, and to appellants' brief (Paper No. 35, filed April 22, 2002) for appellants' arguments thereagainst. Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered. See 37 CFR 1.192(a).

#### OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejection advanced by the examiner, and the evidence of obviousness relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

Upon consideration of the record before us, we reverse, essentially for the reasons set forth by appellants.

We begin with independent claim 36. In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596,

1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785,

788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

The examiner's position (answer, pages 4-6) is that Hagqvist does not disclose that the delay value can be stored as an instruction. To overcome this deficiency in Hagqvist, the examiner turns to Morrison for a teaching that delay value or firing time is well known, and provides intelligence to the instruction stream. In the examiner's opinion, one of ordinary skill in the art would have realized that by adding this extra intelligence to the instructions, processing can be streamlined and resources can be properly utilized. The examiner asserts that it would have been obvious to provide Hagqvist's data processing system with a firing time mechanism as taught by Morrison, because doing so would have provided a mechanism for adding intelligence to the instruction stream at the object code level. Appellants assert (brief, page 6) that "[i]t is respectfully submitted that the Examiner is only selecting bits and pieces from the references without considering the remaining teachings of those references which would lead away from the claimed invention. Furthermore, it is respectfully submitted that the Examiner is misinterpreting *Morrison et al.* and impermissibly modifying *Hagqvist et al.* In light of Applicants[']

teachings." It is argued (brief, page 8) that Hagqvist merely discloses a CPU which is fed address values, and that "nothing in Hagqvist et al. shows, teaches or suggests a delayed instruction includes a field for specifying a delay value and a first program counter value is specified by the field of the delayed instruction as the delay value as claimed in claim 36." It is further argued (brief, page 10) that Morrison merely discloses totally coupling each processor element to a register during its particular instruction firing time such that the instruction firing time indicates the instruction execution timing. Appellants assert (id.) that nothing in Morrison shows, teaches or suggests that the registers are for holding the value to be compared with the program counter, and (brief, page 11) that "Morrison et al. does not show, teach or suggest a delayed instruction, decoding a delayed instruction or determining a coincidence between a value of a program counter and a first program counter value specified by the field of a delay instruction as a delay value as claimed in claim 36."

From our review of Hagqvist and Morrison we find that Hagqvist is directed to a system for enabling a microprocessor to efficiently branch to an alternate program source when a portion of the program is superseded (col. 1, lines 8-10). As shown in

the figure, CPU 10 will normally access addresses 1-200 from operating program 15 and executes them in serial fashion. Each time an address is accessed, program counter 28 is incremented to a next value. Assume that addresses 101-125 in ROM 14 have been replaced by addresses 301-325 in auxiliary storage module 20. When program counter 28 manifests a value 101, that value is determined by address comparator 22 to match a prestored value of 101. As a result, comparator 22 issues a control signal to program counter load controller 26 which causes a program count of 301 to be written from branch control register 24 into program counter 28. CPU 10 then responds to program count 301 by accessing, via I/O module 18, address 301 in auxiliary storage module 20. When program counter 28 reaches address 325, that value is passed to comparator 22 into which value 325 has been has been previously loaded. Upon determining a match, address comparator 22 issues a signal to program counter load control 26 which causes a program count of 126 to be loaded from branch register 24 into program counter 28. When CPU next accesses program counter 28, address value 126 is outputted into line 30. CPU 10 thus accesses address 126 in operating program 15 in ROM 14. The program then continues down the remaining addresses in operating program 15 until its termination (col. 3, lines 23-51).

We find from the disclosure of Hagqvist that when a predetermined address location is reached, the processor branches to an auxiliary memory, and when the data is read out of the auxiliary memory, the processor returns to the main memory to continue executing the main program. Accordingly, we find that Hagqvist does not disclose a delayed function having a field for specifying a delay value, as advanced by the examiner.

Turning to Morrison, we find that Morrison is directed to parallel processing low level instructions having natural concurrences (col. 1, lines 11-15). The invention is directed to a non-Von Neumann type computer system that is capable of using multiple-instruction, multiple data (MIMD) data streams in single context or multiple context (col. 1, lines 36-40). Intelligence is added to the instruction stream at essentially the object code level. The added intelligence can include a logical processor number and an instruction firing time to provide time-driven decentralized control (col. 4, lines 9-19). TOLL software 110 provides synchronization for the system by assigning appropriate firing times to each object code instruction in the output instruction stream (col. 7, line 67 through col. 8, line 2, and col. 12, line 40-42). The software, according to the invention, maps the object code program onto the hardware of the system so

that it executes more efficiently than is typical of prior art systems (col. 6, lines 55-58).

From these teachings of the prior art, we find no teaching or suggestion to provide the system of Hagqvist with firing instructions as taught by Morrison. As acknowledged by the examiner (answer, page 5) Hagqvist does not disclose that the delay value can be stored as part of the instruction, but rather is directed to branching from memory 15 to auxiliary memory 20 in response to a match occurring in comparator 22 when the program count output of program counter 28 matches the pre-loaded address in address comparator 22. In Hagqvist, at the termination of the branch program, program counter 28 reaches the end count of the substitute program. When that value issues on line 32, address comparator 22 (which has been loaded with the end count value) recognizes a match and causes program counter load controller 26 to load a next address value in operating program 15 into program counter 28. This results in CPU 10 accessing the next address value in operating program 15 and continues to run in seamless fashion (col. 2, line 50 through col. 3, line 18). Because Hagqvist is directed to branching from a memory to a substitute memory when the program count reaches a particular address, we find no suggestion that would have motivated an artisan to apply

the firing time mechanism of Morrison to Hagqvist. We do not agree with the examiner's statement (answer, page 5) that "Hagqvist also discloses the delay value that tells execution unit when to execute that instruction and that delay value is stored in a register" but rather find that Hagqvist discloses a branch address value, not a delay value. Moreover, we are not persuaded by the examiner's assertion (answer, pages 5 and 6) that the modification would have been obvious "because doing so would have provided [a] mechanism for adding intelligence to [the] instruction stream at the object code level." We find no motivation for an artisan to modify Hagqvist to add intelligence at the object code level in Hagqvist, other than from use of appellants' disclosure as a template to reconstruct appellants' invention.

"Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983)). "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed

invention is rendered obvious." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992) (citing In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991)).

Because Haggqvist does not address having a delay value for an instruction, and in our view, would not benefit from having a delay value for the instructions, we are not persuaded that the teachings from the applied prior art would have suggested the claimed limitations.

From all of the above, we find that the examiner has failed to establish a prima facie case of obviousness of claim 36. Accordingly, the rejection of claim 36, and claims 37 and 39-42 dependent therefrom, under 35 U.S.C. § 103(a) is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 36, 37 and 39-42 under 35 U.S.C. § 103(a) is reversed.

REVERSED

LEE E. BARRETT	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
LANCE LEONARD BARRY	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
STUART S. LEVY	)	
Administrative Patent Judge	)	

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