Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte MICHAEL WAYNE BLAZIERT and FRANK MARTIN STEPHAN

Appeal No. 2002-2134
Application No. 09/250,481

ON BRIEF

Before STAAB, NASE, and BAHR, Administrative Patent Judges.
NASE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 to 3, 7, 8, 19 to 21, 23 and 24. Claims 5, 6 and 13 to 18 have been canceled. Claims 4, 9 to 12 and 22 are either withdrawn from consideration according to the appellants (reply brief, p. 2) or canceled according to the examiner (answer, p. 2).[1]

We REVERSE.

[1] The examiner and the appellants should resolve this matter upon return of jurisdiction of this application to the examiner.

BACKGROUND

The appellants' invention relates to a method of bending portions of a single circuit board so that integral portions of a single circuit board lie in different planes (specification, p. 1). A copy of the claims under appeal is set forth in the appendix to the appellants' brief.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Wang et al. (Wang)	5,419,038	May 30, 1995
Weber	5,622,588	Apr. 22, 1997
Sakai	6,151,775	Nov. 28, 2000

Claims 1 to 3, 19 to 21, 23 and 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wang.

Claim 7 stands rejected under 35 U.S.C. § 103 as being unpatentable over Wang in view of Weber.

Claim 8 stands rejected under 35 U.S.C. § 103 as being unpatentable over Wang in view of Sakai.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the answer (Paper No. 15, mailed May 31, 2002) for the examiner's complete reasoning in support of the rejections, and to the brief (Paper No. 13, filed May 21, 2002) and reply brief (Paper No. 16, filed July 29, 2002) for the appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

The anticipation rejection

We will not sustain the rejection of claims 1 to 3, 19 to 21, 23 and 24 under 35 U.S.C. § 102(b).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir.), cert. denied, 484 U.S. 827 (1987). The inquiry as to whether a reference

anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 (1984), it is only necessary for the claims to "'read on' something disclosed in the reference, i.e., all limitations of the claim are found in the reference, or 'fully met' by it."

Claims 1 and 19, the independent claims on appeal, read as follows:

1. A method of forming a circuit board with electronic assemblies lying in different planes, comprising:
providing said circuit board with said electronic assemblies and a connecting lead thereon;
forming a channel in a surface of said circuit board opposite said connecting lead, said channel dividing said circuit board into a first portion and a second portion; and
bending said circuit board at said channel so that said second portion is at an angle of between 0 and 180 degrees relative to said first portion.

19. A method of forming a circuit board with electronic assemblies lying in different planes, comprising:
providing said circuit board with said electronic assemblies thereon, at least one channel of a predetermined depth in a first surface of said circuit board, and a connecting lead on a second surface of said circuit board opposite said at least one channel, said at least one channel dividing said circuit board into first and second portions, said connecting lead electrically interconnecting a first of said electronic assemblies on said first portion with a second of said electronic assemblies on said second portion; and
bending said circuit board at said at least one channel between said first and second portions of the circuit board so that said first portion is displaced between 0 and 180 degrees from said second portion.

Wang's invention provides a means for interconnecting two or more electrical components having different planes of orientation. Figure 1 shows a perspective view of two multi-chip modules 10 that are electrically connected to each other by a three dimensional thin-film electrical interconnector 12 constructed according to principles of Wang's invention. The multi-chip modules (MCM) may each comprise a number of integrated circuits or the like that each require electrical connection with a printed circuit board or other MCM. For purposes of reference, the surface of the MCM located at the top portion of Figures 1 and 2 will be referred to as the front side and the surface of the thin-film interconnector adjacent to the MCM front side will be referred to as the front side throughout this description. The surface opposite the front side of the thin-film interconnector will be referred to as the back side throughout this description.

Wang's thin-film interconnector 12 comprises two connectors 14 that are connected to each other by a plurality of electrically conductive wires 16 extending outwardly and away from adjacent faces of each connector. The wires are made from electrically conductive materials and facilitate the transfer of electrical signals and/or power between the connectors 14.

Wang teaches (column 3, line 21, to column 4, line 18)

> a method for fabricating a three dimensional thin-film interconnector that permits electrical connection between two or more electrical components that are

positioned at different planes of orientation and have a high density of electrical connections. The thin-film interconnector is manufactured by depositing a dielectric layer onto the surface of a substrate. A electrically conductive signal plane is deposited onto the surface of the dielectric layer at selected locations that are electrically isolated from each other. A second dielectric layer similar to the preceding dielectric layer is deposited onto the surface of both the signal plane and the portions of the preceding dielectric layer residing between the deposited portions of the signal plane.

A plurality of through holes are formed in the second dielectric layer that extend from the surface of the dielectric layer to the preceding signal plane. The number and arrangement of the through holes are determined according to the electrical connection requirements of the particular electrical components. The through holes are filled with electrically conductive material to form vias. The sequence of depositing a dielectric layer, selectively depositing signal planes, forming a plurality of through holes, and filling the plurality of through holes may be repeated until a predetermined arrangement of signal planes and vias are obtained.

Each signal plane is deposited onto a selected portion of the preceding dielectric layer. The interdigitated sequence of signal planes and dielectric layers in each selected portion make up a signal plane set. The thin-film interconnector comprises at least two connectors that each comprise a signal plane set. If desired, a ground plane may be substituted for a signal plane during the above mentioned sequence. The ground plane comprises an electrically conductive material that serves to minimize any unwanted electromagnetic effects that may otherwise be caused by signal planes in close proximity to one another. However, unlike a signal plane, the ground plane does not require electrical connection with a via.

After the predetermined arrangement of signal planes and vias are obtained, a plurality of contact pads are deposited onto the surface of a final dielectric layer forming the front side surface. The contact pads are deposited at locations corresponding to a plurality of vias in the uppermost signal plane set. Each contact pad is electrically connected to a via which is electrically connected with a signal plane. A plurality of wires are selectively deposited onto the surface of the final dielectric layer. The wires are deposited so that each wire forms an electrical connection between contact pads that are electrically connected to a signal plane set of one connector and the corresponding contact pads that are electrically connected to a signal plane set of another connector.

> The wires extend between the contact pads of each connector across an intermediate body comprising the substrate and the dielectric layers. The intermediate body is removed so that the connectors are mechanically and electrically connected to each other by the plurality of wires. The flexible wire connection between corresponding connectors allows the thin-film interconnector to accommodate electrical connection with electrical components positioned in different planes of orientation.

The appellants argue through both briefs that independent claims 1 and 19 are not anticipated by Wang's completed thin-film interconnector 12 (see Figures 1, 2, 7 and 9-12). We agree. In that regard, we consider Wang's completed thin-film interconnector (i.e, after the intermediate body has been removed, forming the connectors 14 that are electrically and mechanically connected to each other by only the plurality of wires 16) to constitute two circuit boards (i.e., connectors 14) interconnected by a plurality of wires 16. As such, Wang's completed thin-film interconnector does not have a channel formed in a surface of a circuit board as recited in claims 1 and 19.

Since all the limitations of claims 1 and 19 are not disclosed in Wang for the reasons set forth above, the decision of the examiner to reject independent claims 1 and 19, and claims 2, 3, 20, 21, 23 and 24 dependent thereon, under 35 U.S.C. § 102(b) is reversed.

The obviousness rejections

We have reviewed the references to Weber and Sakai additionally applied in the rejection of claims 7 and 8 (dependent on claim 1) but find nothing therein which makes up for the deficiencies of Wang discussed above regarding claim 1. Accordingly, we cannot sustain the examiner's rejection of appealed claims 7 and 8 under 35 U.S.C. § 103.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1 to 3, 19 to 21, 23 and 24 under 35 U.S.C. § 102(b) is reversed and the decision of the examiner to reject

claims 7 and 8 under 35 U.S.C. § 103 is reversed.

REVERSED

LAWRENCE J. STAAB Administrative Patent Judge	)
JEFFREY V. NASE Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
JENNIFER D. BAHR Administrative Patent Judge	)

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