

UNITED STATES PATENT AND TRADEMARK OFFICE

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Ex parte HANS JURGEN MATT, DIETER KOPP,
MICHAEL TROMPF, and STEFAN SPATH

Appeal No. 2002-1938
Application No. 09/292,959

ON BRIEF

Before BARRETT, GROSS, and BARRY, *Administrative Patent Judges*.
BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

A patent examiner rejected claims 1 and 2. The appellants appeal therefrom under 35 U.S.C. § 134(a). We reverse.

BACKGROUND

The invention at issue on appeal concerns the use of a digital signal processor ("DSP") in an application specific integrated circuit ("ASIC"). According to the appellants, a DSP has been used "for various language coding applications as the core of an ASIC." (Paper No. 7 at 1.) Although the computing capacity of the DSP is needed "primarily for special, customer oriented applications," (*id.* at 2), they explain

that "approximately 25% of the computing capacity" is used for routine tasks. (*Id.* at 1-2.) Even if the routine tasks were done by separate modules, add the appellants, "the task of controlling the data transfer from and to the modules must still be handled by the [digital] signal processor which would further impair its computing capacity." (*Id.* at 2.)

Consequently, an object of the invention is to "optimize . . . the computing capacity" of a DSP operating in an ASIC. (Spec. at 2.) More specifically, the ASIC features a router connected between the DSP and other modules in the ASIC. The router controls the transfer of data between the DSP and the other modules "without blocking computing time of the processor." (Paper No. 7 at 2.) Because the DSP is freed from having to control the data transfer, its computing capacity is conserved for performing "more primary tasks." (*Id.*)

A further understanding of the invention can be achieved by reading the following claim.

1. A single integrated circuit comprising:

a processor for processing data,

at least two modules each for processing data packets selected by the processor according to a respective different operation process, and

a router connected between all of said modules and the processor for the purpose of controlling flow of data between the processor and the modules.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,128,509 ("Veijola") in view of U.S. Patent No. 5,541,927 ("Kristol").

OPINION

Rather than reiterate the positions of the examiner or the appellants *in toto*, we address the main point of contention therebetween. Acknowledging that "Veijola did not explicitly show his system was a 'single integrated circuit,'" (Examiner's Answer at 5), the examiner asserts, "Veijola showed his integrated circuit (movable station 10, see fig. 11 and fig. 2 for background) comprises at least two modules (applications 70 [and] 72), a DSP 23 and the connectivity layer 41 (connectivity 41 was taught to be the combination of the router 40 and connection layer 42, see col.5, lines 65-67, col.6, lines 1-8)." (*Id.*) The appellants argue, "Veijola does NOT teach the router, DSP and application modules as part of the same integrated circuit." (Reply Br. at 4.)

"Analysis begins with a key legal question -- *what is the invention claimed?*" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest

reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000).

Here, independent claim 1 specifies in pertinent part the following limitations: "[a] single integrated circuit comprising: a processor . . . , at least two modules each for processing data packets . . . , and a router connected between all of said modules and the processor for the purpose of controlling flow of data between the processor and the modules." Giving the independent claim its broadest, reasonable construction, the limitations require a processor, at least two application modules, and a router **all integrated within the same IC.**

Having determined what subject matter is being claimed, the next inquiry is whether the subject matter would have been obvious. "In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993)(citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). "A *prima facie* case of obviousness is established when the teachings from the prior art itself would . . . have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529,

1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, Veijola discloses "a wireless user terminal or mobile station 10, such as but not limited to a cellular radiotelephone or a personal communicator. . . ." Col. 4, ll. 50-53. The mobile station includes a Digital Signal Processor (DSP) 23, col. 5, ll. 9-10; "Value Added Service (VAS) applications 70 and handportable [sic] user interface applications 72," col. 15, ll. 24-26; and a "router layer 40. . . ." Col. 5, l. 67.

Although the reference's DSP, applications, and router layer are components of the same mobile station 10, the examiner fails to show that the components are integrated within the same IC. To the contrary, the router layer resides on a circuit separate from the DSP circuit. Specifically, "[t]he router 40 . . . may reside in the [Master Control Unit] MCU 21," col. 6, ll. 5-6, which is "typically a microprocessor device, col. 5, ll. 8-9, separate from the DSP 23. *Id.* at ll. 7-11.

Furthermore, the examiner fails to allege, let alone show, that the addition of Kristol cures the aforementioned deficiency of Veijola. Absent a teaching or suggestion of a processor, at least two application modules, and a router all integrated within the same IC, the examiner fails to present a *prima facie* case of obviousness. Therefore, we reverse the obviousness rejection of claims 1 and 2.

CONCLUSION

In summary, the rejection of claims 1 and 2 under § 103(a) is reversed.

REVERSED

LEE E. BARRETT
Administrative Patent Judge

ANITA PELLMAN GROSS
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

)
)
)
)
)
) BOARD OF PATENT
) APPEALS
) AND
) INTERFERENCES
)
)
)
)
)

Appeal No. 2002-1938
Application No. 09/292,959

Page 8

SUGHRUE MION ZINN MACPEAK & SEAS
2100 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 200373213