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Paper No. 35

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD AUSTIN BLANCHARD

Appeal No. 2002-1411
Application No. 09/144,535

ON BRIEF

Before WARREN, OWENS and POTEATE, Administrative Patent Judges.
POTEATE, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the examiner's refusal to allow claims 1, 3-15, 17-21 and 32-41.

Claims 22-31 are pending in the application but have been withdrawn from consideration as being drawn to a non-elected invention. Claims 2 and 16 have been canceled.

Claims 1 and 32 are representative of the subject matter on appeal and are reproduced below:

1. A semiconductor device, comprising:

a semiconductor substrate having a first conductivity;

a first doped region in the substrate and having the first conductivity;

a recess disposed in the first region and having a sidewall and a bottom;

a gate insulator disposed on the substrate and extending to the sidewall of the recess;

a gate electrode disposed on the gate insulator;

a body region disposed in a second region beneath the gate electrode, the body region having a second conductivity and being contiguous with the sidewall, the body region being deeper than the recess, and being self-aligned to the bottom of the recess, self-aligned to the gate electrode at its outer perimeter, self-aligned to the sidewall of the recess at its inner perimeter, such that the body region is assured of being generally symmetrical on all sidewalls and to the bottom of the recess and present at the bottom corners of the recess;

a source region disposed in the body region, having the first conductivity, and being contiguous with the sidewall;

a Schottky contact disposed on the bottom of the recess; and

a source metallization disposed on the Schottky contact and the sidewall of the recess.

32. A semiconductor device made by a method comprising:

forming a gate structure on a semiconductor layer that is disposed on a semiconductor substrate, the gate structure exposing a portion of the layer to form an opening;

implanting a first dopant of a first conductivity and a second dopant of a second conductivity through the opening into the exposed portion of the semiconductor layer, such that regions implanted with the first and second dopants are self-aligned to the opening;

after implanting the first and second dopants, recessing the exposed portion of the semiconductor layer, wherein the recessed exposed portion is self-aligned to the opening;

driving the first dopant deeper into the semiconductor layer after recessing the exposed portion;

driving the first dopant deeper into the semiconductor layer than a bottom of the recessed exposed portion such that the first dopant is self-aligned to the exposed portion such that the first dopant is self-aligned to the sidewall of the recess at its inner perimeter and present at the bottom corners of the recess;

after recessing the exposed portion, forming a Schottky contact on a bottom of the exposed portion; and

forming a source metallization on the Schottky contact and a sidewall of the exposed portion.

Appeal No. 2002-1411
Application No. 09/144,535

The references relied upon by the examiner are:

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| Mihara | 4,823,172 | Apr. 18, 1989 |
| Coe et al. (Coe) | 4,904,613 | Feb. 27, 1990 |
| Tanabe et al. (Tanabe) | 5,598,016 | Jan. 28, 1997 |

Grounds of Rejection

1. Claims 1, 3-10, 12-15, 17-21, 32-35 and 37-41 stand rejected under 35 U.S.C. § 112, first paragraph.
2. Claims 40 and 41 stand rejected under 35 U.S.C. § 112, first paragraph.
3. Claims 1, 3-10, 12-15, 17-21, 32-35 and 37-41 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Mihara in view of Coe.
4. Claims 11 and 36 stand rejected under 35 U.S.C. § 103 as unpatentable over Mihara and Coe and further in view of Tanabe.

We reverse as to all four grounds of rejection.¹

¹ Appellant also requests that the Board reverse the examiner's objections to the drawings and specification. See appeal brief, paper no. 30, received November 30, 2001, page 5, issue no. 1. However, as indicated by the examiner, this issue relates to petitionable subject matter under 37 CFR 1.181 and is not appealable subject matter. See, examiner's answer, paper no. 31, mailed January 15, 2002, page 3, paragraph (6).

Background

The invention relates to a semiconductor device having a Schottky diode and a method of manufacturing the device. Appeal brief, page 2. According to appellant, "[t]he inventive semiconductor device has a higher precision for the location of structures with respect to each other in silicon. It thus uses the silicon area more efficiently and permits smaller semiconductor devices that include Schottky diodes than was possible in the prior art." Id., pages 2-3. These advantages are achieved by self-aligning the various structures of the invention to each other when formed, such that the structures are self-aligned in the final completed device. Id., page 5.

Discussion

1. Rejection of claims 1, 3-10, 12-15, 17-21, 32-35 and 37-41 under 35 U.S.C. § 112, first paragraph

It is the examiner's position that there is no support in the specification for a body region being self-aligned to the gate and for a source region being self-aligned to the recess and having a Schottky contact as recited in the claims. Examiner's answer, pages 5-6. In particular, while the examiner concedes that appellant's structure "is formed self-aligned by using one masking structure," the elements of the structure do not

Appeal No. 2002-1411
Application No. 09/144,535

necessarily remain self-aligned. Examiner's answer, page 11 (noting e.g., that doped regions 100, 102 are no longer self-aligned to the recess after heating).

The test for determining compliance with the written description requirement is whether the disclosure of the application as originally filed reasonably conveys to the artisan that the inventor had possession of the later claimed subject matter at the time of the invention, rather than the presence or absence of literal support in the specification for the claim language. See, Vas-Cath Inc. V. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1116-117 (Fed. Cir. 1991); In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983). As explained by the court in Vas-Cath, 935 F.2d at 1563-64, 19 USPQ2d at 1117:

35 U.S.C. § 112, first paragraph, requires a "written description" of the invention which is separate and distinct from the enablement requirement. The purpose of the "written description" requirement is broader than to merely explain how to "make and use"; the applicant must also convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession **of the invention**. The invention is, for purposes of the "written description" inquiry, **whatever is now claimed**

. . . drawings alone **may** be sufficient to provide a "written description of an invention" required by § 112, first paragraph.

In the present case, we are in agreement with appellant that

Appeal No. 2002-1411
Application No. 09/144,535

the specification and claims support his definition of the term "self-aligned" as referring to alignment at a region and that the term does not require that all edges remain in line. See appeal brief, page 15; see also e.g., specification, page 8, lines 17-20 and page 9, lines 1-5.

The term "self-aligned", as defined in the specification and as used in the prior art including Coe, *et al.* cited by the Examiner is a structural limitation that defines the physical position of two or more features with respect to each other. A semiconductor structure is "self-aligned" when different features have a known physical position in relation to a common third feature each time that structure is made. . . . Once a structure is self-aligned, it cannot ever change and become non-self-aligned. Self-aligned is a physical relationship that is created when the product is formed and remains in the structure thereafter.

Appeal brief, page 13.

The rejection is reversed.

2. Rejection of claims 1, 3-10, 12-15, 17-21, 32-35 and 37-41 under 35 U.S.C. § 103 as unpatentable over Mihara in view of Coe

A proper analysis under 35 U.S.C. § 103 requires, inter alia consideration of two factors: (1) whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device or carry out the claimed process; and (2) whether the prior art would also have revealed that in so making or carrying out, those of ordinary

skill would have a reasonable expectation of success. Both the suggestion and the reasonable expectation of success must be founded in the prior art, not in the applicant's disclosure. In re Vaeck, 947 F.2d, 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). For the reasons discussed below, we find that the examiner has failed to establish a reasonable expectation of success in making the claimed semiconductor device if the teachings of Mihara are modified in view of Coe.

The examiner relies on Mihara as disclosing the invention as claimed with the exception that "Mihara does not teach a gate insulator extending to the side wall, and body and source regions being formed self-aligned to the gate at their outer perimeter and self-aligned to the sidewall of the recess at their inner perimeter, respectively." Examiners answer, page 7. The examiner relies on Coe for a teaching of a DMOS device comprising a recess having a gate insulator extending into the sidewall of the recess and having body and source regions being formed self-aligned to the gate at their outer perimeter and self-aligned at the sidewall of the recess at their inner perimeter. Id. The examiner maintains that it would have been obvious to a person of ordinary skill in the art at the time of the invention to have formed self-aligned features in Mihara's device because it is conventional in the art to do so as taught by Coe in order to

Appeal No. 2002-1411
Application No. 09/144,535

simplify processing steps. See id. pages 7-8 and 14-15.

Appellant concedes that Coe teaches self-aligned features, but notes that Coe fails to teach a Schottky contact disposed at the bottom of the recess as required by the claims. Appeal brief, page 17. Coe fails to show or suggest an opening with a self-aligned recess to the opening extending to a semiconductor substrate to provide a Schottky contact. Id., page 18. As correctly pointed out by the examiner, appellant has failed to establish that one of ordinary skill in the art in considering the Mihara device which includes a Schottky diode would have been motivated to have employed the method of Coe which teaches self-aligned features since Coe fails to disclose how to form a self-aligned recess extending to the semiconductor substrate to provide a Schottky contact. Id., page 18.

We are also unpersuaded by the examiner's argument that "although Mihara does not teach forming the source and body regions in a self-aligned manner, figure 5 of Mihara is identical to the claimed structure, because the claimed final structure, as depicted in figure 9, does not include self-aligned source and body regions." Examiner's answer, page 14. The claims are not, as suggested by the examiner, limited to the embodiment shown in figure 9 of the specification. See In re Cruciferous Sprout Litigation v. Sunrise Farms, 301 F.3d 1343, 1348, 64 USPQ2d 1202,

Appeal No. 2002-1411
Application No. 09/144,535

1205 (Fed. Cir. 2002) (quoting Intervet Am., Inc. v. Kee-Vet Labs., Inc., 887 F.2d 1050, 1053, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989) ("[L]imitations appearing in the specification will not be read into claims, and . . . interpreting what is **meant** by a word **in** a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.'"))).

Accordingly, we find that the examiner has failed to establish a prima facie case of obviousness with respect to claims 1, 3-10, 12-15, 17-21, 32-35 and 37-41. The rejection is reversed.

3. The rejection of claims 11 and 36 under 35 U.S.C. § 103 as unpatentable over Mihara in view of Coe and further in view of Tanabe

Claims 11 and 36 depend from independent claims 1 and 32, respectively. Tanabe is relied on solely for disclosure of a Schottky contact comprising platinum silicide. See appeal brief, page 18; examiner's answer, page 10. Having found that claims 1 and 32 are patentable over Mihara and Coe and, further, that Tanabe fails to remedy the deficiencies in the teachings of Mihara and Coe, we conclude that dependent claims 11 and 36 are patentable over the combined teachings of Mihara, Coe and Tanabe.

The rejection of claims 11 and 36 is reversed.

Appeal No. 2002-1411
Application No. 09/144,535

REVERSED

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| CHARLES F. WARREN |) | |
| Administrative Patent Judge |) | |
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| TERRY J. OWENS |) | APPEALS AND |
| Administrative Patent Judge |) | INTERFERENCES |
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Appeal No. 2002-1411
Application No. 09/144,535

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