

UNITED STATES PATENT AND TRADEMARK OFFICE

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Ex parte MERWIN H. ALFERNESS, MARK D. AUBEL, and FREDERICK H. HATHAWAY

Appeal No. 2002-1395
Application No. 08/789,702

ON BRIEF

Before BARRY, BLANKENSHIP, and SAADAT, *Administrative Patent Judges*.
BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

A patent examiner rejected claims 1-51. The appellants appeal therefrom under 35 U.S.C. § 134(a). We affirm-in-part.

BACKGROUND

The invention at issue on appeal provides hierarchy or modularity to a behavioral description of an integrated circuit ("IC"). (Spec. at 1.) The design of an IC is commonly specified at the register transfer level using a behavioral description. (*Id.* at 2.) Employing hierarchial design techniques to describe the selection and interconnection of an IC's logic or memory components is often desirable. Such design

techniques describe the IC's functionality at various levels of abstraction, ranging from the most general function performed by the IC to the specific function performed by each logic and memory component thereof. (*Id.* at 1-2.)

The appellants assert that a hierarchical design can be stored efficiently by providing "modularity" to a circuit design database. Modularity refers to representing identical functions in a design with multiple instances of a common component. For example, a common adder bit slice may be described using a behavioral language, and the resulting behavioral description may be stored as an adder bit slice module in a design library. When a N-bit adder is desired, a circuit designer instantiates "N" adder bit slice modules. Each adder bit slice instance within the design may reference the behavioral description for the common adder bit slice module. Although modularity may be provided without providing hierarchy, and vice versa, modularity and hierarchy are typically provided together. (*Id.* at 3.)

The appellants' invention provides hierarchy or modularity to a behavioral description of an IC by using a template for a selected portion of the IC's design. The template comprises a template call and a corresponding template behavioral description; the template is instantiated in the behavioral description of the circuit design by including the template call therein. The behavioral description may then be

expanded using an expander preprocessor. More specifically, the preprocessor incorporates the behavioral description of the template into the behavioral description of the IC and provides template markers to identify the location of the template. (*Id.* at 9.)

A further understanding of the invention can be achieved by reading the following claim.

1. A method for providing a behavioral description of a circuit design, the method comprising the steps of:

a. providing a template behavioral description, wherein the template behavioral description models a selected portion of the circuit design; and

b. instantiating a template call in the behavioral description of the circuit design by incorporating the template call into the behavioral description of the circuit design, the template call referencing the corresponding template behavioral description.

Claims 1-51 stand rejected under 35 U.S.C. § 112, ¶ 2, as indefinite. Claims 1-51 also stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,987,239 ("Kirsch"). The same claims stand rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,572,437 ("Rostoker") and U.S. Patent No. 5,625,565 ("Van Dyke").

OPINION

Our opinion addresses the rejections in the following order:

- indefiniteness rejection
- anticipation rejection
- obviousness rejection.

Indefiniteness Rejection

Rather than reiterate the positions of the examiner or the appellants *in toto*, we address the two points of contention therebetween. First, the examiner asserts, "[r]elatively flat in claim 13 is ambiguous (this is also present in claims 14-15, 48-50)." (Examiner's Answer at 5.) The appellants argue, "further limitation of claim 13 is not deemed necessary in the absence of cited prior art." (Appeal Br.¹ at 26.) They cite "page 45, lines 1-2" of their specification as corresponding to claims 13 and 48. (*Id.* at 18-19).

"Definiteness problems often arise when words of degree are used in a claim." *Seattle Box Co. v. Indus. Crating & Packing, Inc.*, 731 F.2d 818, 826, 221 USPQ 568, 573 (Fed. Cir. 1984). "When a word of degree is used, such as the term 'relatively', it is

¹We rely on and refer to the second supplemental appeal brief, (Paper No. 13), in lieu of the original appeal brief, (Paper No. 8), and the first supplemental appeal brief, (Paper No. 11), because the latter two briefs were defective. (Paper Nos. 9, 12.) The original appeal brief and the first supplemental appeal brief were not considered in deciding this appeal.

necessary to determine whether a specification provides some standard for measuring that degree." *Ex parte Oetiker*, 23 USPQ2d 1651, 1654 (Bd. Pat. App. & Int. 1990) (citing *Seattle Box Co.*, 731 F.2d at 826, 221 USPQ at 574), *aff'd*, 951 F.2d 1267, 23 USPQ2d 1661 (Fed. Cir. 1991).

Here, the specification provides no standard for measuring a degree of relative flatness. The passage of the specification cited by the appellants merely uses a different word of degree, viz., "effectively," (Spec. at 45); It does not indicate how the claimed "detailed description" relates to or differs from detailed descriptions that are not relatively flat. Absent such a standard or indication, the claims read in light of the specification fail to apprise one skilled in the art of the scope of the invention. Therefore, we affirm the indefiniteness rejection of claims 13-15 and 48-50.

Second, the examiner asserts, "[t]he term 'template' in the claims is used by the claim to mean 'that defined in lines 5-11, page 9, specification,' while the accepted meaning is 'that given in col. 1, line 65 to col. 2, line 5 of Van Dyke.' The Examiner can not [sic] distinguish between the two definitions." (Examiner's Answer at 5.) The appellants argue, "[t]hough Applicants do not understand the rejection, it is their position that their definition and use of the term 'template' comports with the requirements of MPEP 2173.05 (a)." (Appeal Br. at 24.)

"The test for definiteness is whether one skilled in the art would understand the bounds of the claim when read in light of the specification. *Orthokinetics Inc., v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986). If the claims read in light of the specification reasonably apprise those skilled in the art of the scope of the invention, Section 112 demands no more. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1385, 231 USPQ 81, 94 (Fed. Cir. 1986)." *Miles Labs., Inc. v. Shandon Inc.*, 997 F.2d 870, 875, 27 USPQ2d 1123, 1126 (Fed. Cir. 1993).

Here, the examiner admits that "[t]he term 'template' in the claims is used by the claim to mean 'that defined in lines 5-11, page 9, specification,' . . ." (Examiner's Answer at 5.) This passage of the appellants' specification explains that a template is provided "for a selected portion of the circuit design," (Spec. at 9), to "selectively provid[e] modularity to a behavioral description of a circuit design. The template includes a template call and a corresponding template behavioral description." (*Id.*) Claim 1² explains that the template behavioral description "models a selected portion of

²"The claims as filed are part of the specification, and may provide or contribute to compliance with Section 112." *Hyatt v. Boone*, 146 F.3d 1348, 1352, 47 USPQ2d 1128, 1130 (Fed. Cir. 1998) (citing *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 938, 15 USPQ2d 1321, 1326 (Fed. Cir. 1990); *In re Benno*, 768 F.2d 1340, 1346, 226 USPQ 683, 686-87 (Fed. Cir. 1985); *In re Frey*, 166 F.2d 572, 575, 77 USPQ 116, 119 (CCPA 1948)).

the circuit design" and that the template call "referenc[es] the corresponding template behavioral description." The specification explains that "[t]he template is instantiated in the behavioral description of the circuit design by including the template call therein."

(Spec. at 9.)

In light of these explanations, we conclude that one skilled in the art would understand that the claimed template comprises a definition of part of a circuit and a reference to the definition incorporated into a description of the circuit. Therefore, we reverse the indefiniteness rejection of claims 1-12, 16-47, and 51.

Anticipation Rejection

"[T]o assure separate review by the Board of individual claims within each group of claims subject to a common ground of rejection, an appellant's brief to the Board must contain a clear statement for each rejection: (a) asserting that the patentability of claims within the group of claims subject to this rejection do not stand or fall together, and (b) identifying which individual claim or claims within the group are separately patentable and the reasons why the examiner's rejection should not be sustained." *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002 (citing 37 C.F.R. §1.192(c)(7) (2001))). "Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable." 37 C.F.R.

§ 1.192(c)(7). "If the brief fails to meet either requirement, the Board is free to select a single claim from each group of claims subject to a common ground of rejection as representative of all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim." *McDaniel*, 293 F.3d at 1383, 63 USPQ2d at 1465.

Here, although the appellants allege "that pending claims 1-51 are patentably distinct from one another," (Appeal Br. at 20), they fail to satisfy the second requirement for claims 4-28 and 32-51. More specifically, their pointing out differences in what claims these claims cover, (*id.* at 31-50), is not an argument that the claims are separately patentable. Therefore, claims 4-28 and 32-51 stand or fall with representative claim 1.

With this representation in mind, rather than reiterate the positions of the examiner or the appellants *in toto*, we address the five points of contention therebetween. First, the examiner asserts, "Kirsch discloses macros [col. 1, line 66 to col. 2, line 38; col. 3, line 20 to col. 4, line 50. Note the example of a macro [col. 4] for a decoder. . . ." (Examiner's Answer at 16.) The appellants argue, "[n]one of the prior art even suggests a 'template behavioral description'. None certainly combines this with 'instantiating a template call in the behavioral description'." (Appeal Br. at 29.)

"Analysis begins with a key legal question -- *what* is the invention *claimed*?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)).

Here, claim 1 specifies in pertinent part the following limitations: "providing a template behavioral description, wherein the template behavioral description models a selected portion of the circuit design; and . . . instantiating a template call in the behavioral description of the circuit design by incorporating the template call into the behavioral description of the circuit design, the template call referencing the corresponding template behavioral description." Giving the representative claim its broadest, reasonable construction, the limitations require defining part of a circuit and incorporating a reference to the definition into a description of the circuit.

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous*

Sprout Litig., 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002).

"[A]nticipation is a question of fact." *Hyatt*, 211 F.3d at 1371, 54 USPQ2d at 1667 (citing *Bischoff v. Wethered*, 76 U.S. (9 Wall.) 812, 814-15 (1869); *In re Schreiber*, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997)). "A claim is anticipated . . . if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 715, 223 USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)).

Here, Kirsch discloses "a computer system 10 for designing control logic for a complex digital system represented in a hardware description language. . . ." Col. 2, l. 66 - col. 3, l. 2. We find that the computer system defines part of a circuit in "a plurality of macro files 13." Col. 3, l. 29. More specifically, "macro files 13 can be used . . . to store macro definitions for related control logic operations as instruction groups, such as arithmetic, move, branch and program control, bit manipulation, multiplication or special instruction groups." Col. 5, ll. 14-18. Such "[a] macro definition associates the macro name with a particular segment of microcode. . . ." Col. 3, ll. 37-39.

We further find that the reference's computer system incorporates a reference to the definition into a description of the circuit. Specifically, "[a] macro instantiation is simply a reference to a macro name located at a place in the source code file at which a segment of prestored microcode is to be substituted." *Id.* at ll. 34-37. Because the macro instantiation references a macro name, and the macro definition associates the macro name to a segment of microcode, the macro instantiation is a reference to the macro definition (and to the segment of microcode). Therefore, we affirm the anticipation rejection of claim 1 and of claims 4-28 and 32-51, which fall therewith.

Second, observing that claim 2 "is further limited over claim 1 by an 'identifying step' and an 'incorporating step,'" (Appeal Br. at 30), the appellants allege, "none of the prior art of record teaches this combination." (*Id.*)

Claim 2 specifies in pertinent part the following limitations: "identifying the template call in the behavioral description of the circuit design; and . . . incorporating the template behavioral description that corresponds to the template call into the behavioral description of the circuit design." Giving the claim its broadest, reasonable construction, the limitations require identifying the reference in the description of the circuit and incorporating the definition that corresponds to the reference into the description.

Turning to Kirsch, we find that its computer system identifies the references in the description of the circuit, i.e., the macro instantiations in the source code. Specifically, "[a]s . . . shown in FIG. 3 et seq., the preprocessor 14 first locates a macro instantiation. . . ." Col. 5, ll. 27-29. We further find that once a macro instantiation is identified, the preprocessor incorporates the (macro) definition that corresponds to the instantiation into the description. Specifically, if "the line of data instead represents a macro instantiation (block 54), a routine for substituting the macro instantiation with a macro definition, as further described below in FIG. 5, is called. . . ." Col. 6, ll. 53-56. Therefore, we affirm the anticipation rejection of claim 2

Third, the examiner asserts, "Kirsch discloses macros . . . col. 3, line 20 to col. 4, line 50. . . ." (Examiner's Answer at 16.) Observing that "[c]laim 3 is a method claim which depends from claim 2 and further limits the 'behavioral description,' (Appeal Br. at 30, the appellants allege, "[t]his is not taught in any of the prior art of record." (*Id.*)

Claim 3 specifies in pertinent part the following limitations: "the behavioral description of the circuit design is stored in a file. . . ." Giving the claim its broadest, reasonable construction, the limitations require storing the description of the circuit.

Turning to the reference, the aforementioned identification and incorporation is performed by a "preprocessor which replaces all macro instantiations with a microcode segment from the corresponding macro definition to form a final output hardware description language source code file." Col. 8, ll. 21-24. We find that Kirsch stores the final output source code file. Specifically, "[t]he . . . output file 15 [is] stored in the memory." Col. 3, ll. 48-49. Therefore, we affirm the anticipation rejection of claim 3.

Fourth, observing that claim 29 "is further limited by a 'placing step,'" (Appeal Br. at 40), the appellants allege, "the prior art of record does not contain this combination." (*Id.*)

Claim 29 specifies in pertinent part the following limitations: "placing the second one of the hierarchical elements." Giving the claim its broadest, reasonable construction, the limitations require placing at least one hierarchical element.

Turning to Kirsch, we find that the aforementioned complex digital system comprises hierarchical elements. "An example of a complex digital system is a microprocessor characterized by a very large number of logic gates, representing a large finite state machine. . . ." Col. 3, ll. 3-5. In this example, the microprocessor

resides at a higher level of hierarchy than the logic gates. Similarly, the large finite state machine resides at a higher level of hierarchy than the logic gates.

We further find that the reference places at least one of these hierarchical elements. More specifically, "a synthesizer 20 can be used by the designer, using the net list 19 as inputs, to create an integrated circuit layout to be used to fabricate an actual physical electronic circuit chip 21." *Id.* at ll. 61-65. The laying out of the IC involves placing the aforementioned hierarchical elements thereof. Therefore, we affirm the anticipation rejection of claim 29.

Fifth, observing that claim 30 "further limits the 'hierarchical elements,'" (Appeal Br. at 41), the appellants allege, "the prior art of record does not contain this combination." (*Id.*)

Claim 30 specifies in pertinent part the following limitations: "the second one of the hierarchical elements includes a number of sub-elements, whereby the number of sub-elements of the second one of the hierarchical elements are located at the same relative position as the sub-elements of the first one of the hierarchical elements because the second one of the hierarchical elements references the updated common placement database.

"The review authorized by 35 U.S.C. Section 134 is not a process whereby the examiner . . . invite[s] the [B]oard [of Patent Appeals and Interferences] to examine the application and resolve patentability in the first instance." *Ex parte Braeken*, 54 USPQ2d 1110, 1112 (Bd.Pat.App. & Int. 1999). In an *ex parte* appeal, "the Board is basically a board of review — we review . . . rejections made by patent examiners." *Ex parte Gambogi*, 62 USPQ2d 1209, 1211 (Bd.Pat.App. & Int. 2001). Furthermore, "absence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Here, the examiner does not allege, let alone show, that the reference discloses the aforementioned limitations. We will not resort to speculation as to such a possible disclosure. Therefore, we reverse the anticipation rejection of claim 30 and of claim 31, which depends therefrom.

Obviousness Rejection

The examiner quotes the abstract of Rostoker and "[c]ol. 2, line 44 to col. 3, line 62" of Van Dyke. (Examiner's Answer at 7.) The appellants argue, "[n]one of the prior art even suggests a 'template behavioral description'. None certainly combines this with 'instantiating a template call in the behavioral description'." (Appeal Br. at 29.)

As explained regarding the anticipation rejection, claims 1 requires defining part of a circuit and incorporating a reference to the definition into a description of the circuit. Claims 17 and 39, the other independent claims, specify similar limitations.

Having determined what subject matter is being claimed, the next inquiry is whether the subject matter would have been obvious. "In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) (citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). "A *prima facie* case of obviousness is established when the teachings from the prior art itself would . . . have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, the examiner does not allege, let alone show, that teachings from Rostoker and Van Dyke would have suggested defining part of a circuit and incorporating a reference to the definition into a description of the circuit. We will not resort to speculation as to such a possible suggestion. Therefore, we reverse the obviousness rejection of claim 1; of claims 2-16, which depend therefrom; of claim 17; of claims 18-

38, which depend therefrom; of claim 39; and of claims 40-51, which depend therefrom.

"The PTO Rules of Practice require the examiner to cite only what he considers the 'best references.'" *E.I. duPont de Nemours & Co. v. Berkley & Co.*, 620 F.2d 1247, 620 F.2d 1247, 1266-67, 205 USPQ 1, 16 (8th Cir. 1980). "The examiner is not called upon to cite *all* references that may be available, but only the 'best.'" M.P.E.P. § 904.03 (8th ed., rev. 1 Feb. 2003) (quoting 37 C.F.R. § 1.104(c)(2002)). "Multiplying references, any one of which is as good as, but no better than, the others, adds to the burden and cost of prosecution and should therefore be avoided." *Id.*

Here, the examiner's treatment of Rostoker and Van Dyke evidences that the references are no better than Kirsch. The examiner should avoid such multiplication of references.

CONCLUSION

In summary, the rejection of claims 1-12, 16-47, and 51 under § 112, ¶ 2, is reversed, while the rejection of claims 13-15 and 48-50 under § 112, ¶ 2, is affirmed. The rejection of claims 1-29 and 32-51 under § 102(e) is affirmed, while the rejection of claims 30 and 31 under § 102(e) is reversed. The rejection of claims 1-51 under § 103(a) is also reversed.

"Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences. . . ." 37 C.F.R. § 1.192(a). Accordingly, our affirmance is based only on the arguments made in the brief. Any arguments or authorities not included therein are neither before us nor at issue but are considered waived. No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART

LANCE LEONARD BARRY)	
Administrative Patent Judge)	
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