

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* CHARLES CHIUN-CHIEH YANG  
and DARRELL D. WATKINS, JR.

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Appeal No. 2002-0974  
Application 09/332,745<sup>1</sup>

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ON BRIEF

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Before METZ, OWENS and PAWLIKOWSKI, *Administrative Patent Judges*.  
METZ, *Administrative Patent Judge*.

*DECISION ON APPEAL*

This is an appeal under 35 U.S.C. § 134 from the examiner's refusal to allow claims 1 through 38, all the claims in the application.

**THE INVENTION**

The appealed subject matter is directed to a process for preparation of a silicon wafer having an epitaxial layer

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<sup>1</sup> Application for patent filed June 14, 1999.

Appeal No. 2002-0974  
Application 09/332,745

deposited thereon. Appellants' process comprises depositing an epitaxial layer on the surface of a silicon wafer and then heating the wafer to a temperature of at least about 1175°C during and/or after the epitaxial deposition. The wafer is then cooled for a period of time at a rate of at least about 10°C per second while the temperature of the wafer is greater than about 1000°C and while the wafer is not in contact with the susceptor. All the steps of epitaxial deposition, heating and cooling are conducted in the same reactor chamber.

Claim 1 is believed to be adequately representative of the appealed subject matter and is reproduced below for a more facile understanding of the claimed invention:

Claim 1. A process for the preparation of a silicon wafer comprising a surface having an epitaxial layer deposited thereon, the process comprising:

depositing an epitaxial layer onto a surface of a silicon wafer;

heating the wafer to a temperature of at least about 1175°C during and/or after the epitaxial deposition; and

cooling the heated wafer for a period of time at a rate of at least about 10°C/sec while **(a)** the temperature of the wafer is greater than about 1000°C, and **(b)** the wafer is not in contact with a susceptor, wherein the epitaxial deposition, heating, and cooling are conducted in the same reactor chamber.

Appeal No. 2002-0974  
Application 09/332,745

**THE REFERENCES**

The references of record which are being relied on by the examiner as evidence of obviousness are:

Miyashita et al.	5,271,796	December 21, 1993
Nakagawa et al.	5,445,491	August 29, 1995
Loncki et al.	5,860,848	January 19, 1999
Park et al.	5,944,889	August 31, 1999

Japanese Patent Application No. 8-24796, Asayama et al., January 17, 1996<sup>2</sup>

Japanese Published Application No. 2-243594, Inoue et al., September 27, 1990<sup>3</sup>

**THE REJECTIONS**

In his answer, the examiner has withdrawn his rejection of claim 6 as failing to comply with 35 U.S.C. § 112, first paragraph.

Claims 1 through 8 stand rejected under 35 U.S.C. § 103 as being unpatentable because the subject matter therein claimed would have been obvious from the combined disclosures of Asayama et al. considered with Inoue et al. and Nakagawa et al. Claims 9 through 38 stand rejected as being unpatentable under 35 § 103

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<sup>2</sup> Appellants filed two English translations of this reference, one of which was prepared by Derwent Information, Ltd. The examiner has relied on the "non-Derwent" translation and, accordingly, we shall also rely on the "non-Derwent" translation. The translations are, substantially, the same.

<sup>3</sup> All reference to Inoue et al. is a reference to the English translation obtained by the U.S. Patent and Trademark Office (PTO).

Appeal No. 2002-0974  
Application 09/332,745

because the subject matter therein claimed would have been obvious from the combined disclosures of Asayama et al. considered with Inoue et al. and Nakagawa et al. in further view of Loncki et al., Miyashita et al. and Park et al.

#### **OPINION**

We begin by determining the scope and content of appellants' claims because it is the claims which define the protection for which appellants seek a patent. United Carbon Co. v. Binney & Smith Co., 317 U.S. 228, 232, 55 USPQ 381, 383-384 (1942) (citing General Electric Co. v. Wabash Appliance Corp., 304 U.S. 364, 369, 37 USPQ 466, 468-469 (1938); In re Zletz, 893 F.2d 319, 321, 322, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); SRI Int'l. v. Matsushita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 586 (Fed. Cir. 1985) (en banc).

Appellants' process is claimed as a process "comprising" the combination of the various steps recited in the claims. As a "comprising" claim, the claims do not exclude any other process steps or ingredients disclosed in the prior art, including other steps and ingredients disclosed but not claimed by appellants, and those neither disclosed nor even contemplated by appellants. In re Baxter, 656 F.2d 679, 686, 210 USPQ 795, 802 (CCPA 1981).

Thus, the process of claim 1 "comprises" three steps: (1)

Appeal No. 2002-0974  
Application 09/332,745

depositing an epitaxial layer onto the surface of a silicon wafer; (2) heating the wafer to a temperature of at least 1175°C during epitaxial layer deposition, after epitaxial layer deposition or during and after epitaxial layer deposition; and , (3) cooling the heated wafer from the second step for a period of time and at a rate of at least about 10°C per second. The third step is conducted while: the temperature of the wafer is greater than about 1000°C; and, during cooling, the wafer is not in contact with a susceptor. Each of the three process steps of deposition, heating and cooling are conducted in the same reactor chamber.

The epitaxial layer deposited on the surface of the silicon wafer is not set forth in claim 1. While appellants disclose that the layer deposited is epitaxial silicon, claim 1 is not so limited and, therefore, embraces depositing any epitaxial layer. The cooling step requires a cooling rate of at least 10°C per second while the temperature of the wafer is greater than 1000°C. Thus, the claimed process includes cooling the wafer while it is above 1000°C at the specified rate and after the temperature falls below 1000°C cooling at any rate or not cooling at all. According to appellants' disclosure, the cooling may be effected by simply turning off the heat source for the reactor.

Appeal No. 2002-0974  
Application 09/332,745

Additionally, appellants disclose and claim 1 requires that the cooling effected while the temperature is above 1000°C is obtained while the susceptor is withdrawn from the wafer. This has the effect of increasing the cooling rate. When the susceptor is removed the wafer is supported by pins thereby limiting the contact of the wafer with other hot surfaces.

Appellants have chosen to argue the patentability of their claims over the cited references based on patentability of claim 1 as representative of claims 1 through 8 (see page 6 of the brief); claim 9 as representative of claims 9 through 27 (see page 12 of the brief); claim 28 as representative of claims 28 through 33 and 35 through 38 (see page 15 of the brief); and, claim 34 as standing or falling on its own (see page 15 of the brief). After a careful consideration of the entire record before us, we conclude that the examiner has made out a *prima facie* case of obviousness which has not been rebutted. Accordingly, for the reasons which follow, we shall affirm the examiner's rejection.

**THE REJECTION OF CLAIMS 1 THROUGH 8**

The examiner has rejected claims 1 through 8 over the combined disclosures of Asayama et al., Inoue et al and Nakagawa et al. We agree with the examiner that Asayama et al. is evidence that at the time appellants made their invention it would have

been obvious to rapidly cool an epitaxially deposited layer of silicon on a silicon wafer at a rate of at least 10°C per second<sup>4</sup>. While Asayama et al. do not disclose that cooling is effected while the wafer is not in contact with a susceptor, Inoue et al. does disclose that feature and Inoue et al. discloses that the reason for removing the susceptor is to increase the rate of cooling. Neither does Asayama et al. disclose that their process may be effected in a single process chamber but Nakagawa et al. discloses that in an integrated semiconductor manufacturing process including heating, epitaxial growth and cooling, the process may be conducted in a single process chamber. We find that simple process economics and efficiency would have motivated a person of ordinary skill to use the least amount of apparatus necessary to carry out any integrated process comprising multiple steps.

We remind appellants that the question which we address here is what does the combination of references on which the examiner has relied teach and what would the combined teachings have suggested to a person of ordinary skill in the art. In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). We remind

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<sup>4</sup> Asayama et al. describes cooling in terms of degrees Kelvin (K) but we take official notice of the fact that one degree K is the same as one degree C.

Appeal No. 2002-0974  
Application 09/332,745

appellants that in considering the prior art we must presume the routineer is skilled not the contrary. In re Sovish, 769 F.2d 738, 743, 226 USPQ 771, 774 (Fed. Cir. 1985). In this art, the hypothetical person of ordinary skill, the semiconductor manufacturing engineer, would be expected to be well versed in chemistry, engineering and physics. Further, appellants have conceded in their specification that high temperature heat treatments have been used in the prior art to reduce the number density of "crystal originated pits" (COP's) and that epitaxial deposition of thin, crystalline silicon on the wafer surface has also been used in the prior art to produce a wafer free from COP's (see page 2, line 14 through page 3, line 2 of the specification).

We do not find persuasive appellants' arguments concerning Asayama et al.'s disclosed cooling rate of "at least 10K/s" after the growth of the epitaxial layer on the silicon wafer. The temperature at which Asayama et al. begins cooling, between 1150°C and 1250°C meets the limitation in claim 1 that cooling at a particular rate is effected "during and/or after" the epitaxial deposition and when the wafer is "greater than 1000°C." Moreover, since appellants rapidly cool their wafer for the same reason as do Asayama et al., that is, to create internal intrinsic

gettering (**IG**) regions in the wafer and obtain a highly crystallinity active device region, we do not understand Asayama et al. to disclose a different cooling rate than appellants as argued at page 7 of the brief. Moreover, appellants' argument concerning constant versus non-constant cooling is not reflected in the claims. The claims merely require cooling at least 10°C/second as long as the wafer is above 1000°C. This is shown by Asayama et al.

Appellants' arguments concerning Inoue et al.'s disclosure of removing the susceptor from contact with the wafer to improve the cooling rate ignores the level of skill of the routineer. In the first instance, Inoue et al. clearly state that the purpose for removing the susceptor from the wafer is to increase the cooling rate, the very same reason appellants remove the susceptor from the wafer in their process. Indeed, we think rudimentary knowledge of the laws of thermodynamics would suggest that removing a hot, relatively large mass away from another hot but relatively smaller mass would increase the rate at which the smaller mass cooled.

Appellants' argument concerning Inoue et al.'s lack of disclosure concerning the composition of the epitaxial layer and the single crystal substrate in their process ignores the

rejection before us and the scope of claim 1. Asayama et al. discloses both the nature of the epitaxial layer and the wafer and the rejection is, again, over the combined disclosures of Asayama et al., Inoue et al. and Nakagawa et al. Further, claim 1 is not limited to a single crystal substrate and claim 1 does not set forth any particular epitaxial layer. Also, as a "comprising" claim, claim 1 does not exclude Inoue et al.'s steps of increasing and decreasing the temperature in their process.

We find that when the prior art is considered in light of the level of skill possessed by the semiconductor manufacturing engineer it fairly suggests the claimed process. We consider that the examiner has provided evidence in the nature of the prior art on which he has relied which establishes that the claimed subject matter would have been *prima facie* obvious at the time appellants made their invention. Accordingly, we find absolutely no merit in appellants' argument that the examiner has impermissibly relied on appellants' disclosure as a guide for combining the proffered prior art. Appellants perform the same steps as Asayama et al. and for the same reason. Conducting the process of Asayama et al. in the manner suggested by Inoue et al. to increase the cooling rate and in a single reaction chamber as disclosed by Nakagawa et al. for process efficiency and economics would have been obvious

Appeal No. 2002-0974  
Application 09/332,745

to the hypothetical person of ordinary skill in the art at the time appellants' made their invention.

**THE REJECTION OF CLAIMS 9 THROUGH 38**

Appellants argue that claim 9 requires a wafer exhibiting "an average light scattering event concentration of at least 0.5/cm<sup>2</sup>" and that no reference discloses starting with a wafer having this property. We disagree. We consider the limitation in claim 9 concerning the minimum concentration of light scattering events on the surface of the wafer at the beginning of the process to be inherent in the wafers disclosed by Asayama et al. for use in their process. Specifically, appellants disclose at page 8, lines 19 through 21 of their specification that:

The wafer starting material preferably is a single crystal silicon wafer which has been sliced from a single crystal ingot grown in accordance with any of the conventional variations of the Cz crystal growing method.

These are the so-called "void-rich wafer" materials to which appellants refer in their specification and which contain a relatively large number of "vacancy agglomerates" (see page 1, lines 17 through 25 and page 10, lines 3 through 23). When these "agglomerates" are found at the surface of the wafer, they appear in the form of COP's and the COP's are detected as "light scattering events" on the surface. According to appellants:

Void-rich wafers are particularly preferred starting

Appeal No. 2002-0974  
Application 09/332,745

materials because they may be sliced from silicon ingots formed by relatively low-cost processes, e.g., the traditional open-architecture Cz process.

See page 10, lines 21 through 23 of the specification. But, Asayama et al. specifically recognize that silicon wafers prepared by the Cz process are conventionally used in highly integrated semiconductor devices and Asayama et al. uses silicon wafers in their process which are prepared using the Cz process. Accordingly, there exists a reasonable factual basis to presume that because appellants use silicon wafers prepared by the same method as Asayama et al. prepare the silicon wafers for their process that the wafers have the same or at least substantially the same surface characteristics.

We have not overlooked appellants' argument that "oxygen-related crystal defects are distinguishable from the light-scattering events required by claim 9" (see page 13 of the brief) but there is no underlying evidence which supports appellants' argument. Further, the argument does not address the fact that appellants, like Asayama et al., prepare their silicon wafer from single crystal ingots prepared according to the Cz method. Accordingly, although we agree with the examiner that Miyashita, Park and Loncki are evidence of the ordinary level of surface imperfections which may typically be found in single crystal

silicon wafers prepared by the Cz process, we find that the references are not necessary to sustain the rejection before us because appellants prepare their silicon wafers using the same process as Asayama et al. use to prepare their wafers.

It is not entirely clear from appellants' arguments concerning the alleged separate patentability of claim 28 what is the limitation in claim 28 which renders it separately patentable from appellants' other claims. It is not an adequate "argument" to simply point out what the claim covers or how it differs from the prior art. It is necessary to explain why the differences between what is claimed and the prior art would not have been obvious in the sense of § 103. Nevertheless, it appears that it is the limitation concerning the thickness of the epitaxial layer in claim 28 which appellants believe sets claim 28 apart from the prior art. That is, claim 28 requires an epitaxial layer of at least about 0.1  $\mu\text{m}$  and less than 3  $\mu\text{m}$ . But Asayama et al. discloses depositing epitaxial layers "approximately 3  $\mu\text{m}$  thick" on their silicon wafers. See paragraph 18, last sentence. That disclosure meets the limitation in claim 28 because "approximately 3  $\mu\text{m}$ " would have been understood to mean slightly more than or slightly less than 3  $\mu\text{m}$ . Also note that Inoue et al. discloses depositing epitaxial layers of **GaAs** of from 1 to 2

Appeal No. 2002-0974  
Application 09/332,745

$\mu\text{m}$  on a silicon wafer. Claim 28 is not limited to any particular epitaxial layer but is directed to "an epitaxial layer."

Similarly, at pages 15 and 16 of their brief appellants recite the various limitations in claim 34 (epitaxial layer thickness, heating and cooling, surface condition of the wafer, etcetera) and then proclaim that the office has not made out a *prima facie* case of obviousness with respect to the subject matter claimed in claim 34. We find appellants' "argument" lacks adequate specificity to establish what constitutes the error in the proffered rejection. Suffice it to say that, for reasons expressed fully above, we find the examiner has made out a *prima facie* case of obviousness with respect to the subject matter of claim 34.

Having concluded that the examiner has made out a prima facie case of obviousness with respect to the appealed subject matter, it is necessary for us to consider appellants' rebuttal evidence, if any, and to reconsider the prima facie case anew in light of all the evidence. In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). However, appellants have neither presented any rebuttal evidence nor advanced any arguments with respect to any probative showing of surprising or unexpected results represented by objective evidence in this

Appeal No. 2002-0974  
Application 09/332,745

record. Accordingly, on this record the *prima facie* case of obviousness stands unrebutted.

**SUMMARY**

The examiner's rejection of claims 1 through 38 as being unpatentable under 35 U.S.C. § 103 is **affirmed**.

The decision of the examiner is **affirmed**.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

**AFFIRMED**

ANDREW H. METZ )  
Administrative Patent Judge )  
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TERRY J. OWENS ) BOARD OF PATENT  
Administrative Patent Judge ) APPEALS AND  
) INTERFERENCES  
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BEVERLY A. PAWLIKOWSKI )  
Administrative Patent Judge )

Appeal No. 2002-0974  
Application 09/332,745

AHM/gjh

SENNIGER, POWERS, LEAVITT AND ROEDEL  
ONE METROPOLITAN SQUARE  
16TH FLOOR  
ST. LOUIS, MO 63102