

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte CARL L. BOWEN and KEITH Q. LAO

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Appeal No. 2001-2503  
Application No. 09/075,767<sup>1</sup>

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ON BRIEF

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Before PAK, WALTZ and JEFFREY SMITH, Administrative Patent Judges.

PAK, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 from the examiner's refusal to allow claims 1, 2, 4-10, 12-16 and 18-47, which are all the claims pending in this application. Claims 1, 9, 15, 23, 30 and 35 have been amended after the final Office action dated July 5, 2000.

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<sup>1</sup> Application for patent filed May 11, 1998.

APPEALED SUBJECT MATTER

The subject matter on appeal is directed toward a method of forming a semiconductor device comprising a fuse and an integrated circuit wherein a contact pad is formed above the integrated circuit. See e.g., claims 1, 15 and 35. The method involves, *inter alia*, patterning an anti-reflective coating formed on the contact pad while simultaneously removing a dielectric material that was deposited over the fuse. *Id.* This method requires that the anti-reflective coating and the dielectric material be etched at “substantially the same rate”, i.e., an etch rate selectivity of approximately 1:1. See e.g., claims 1, 15 and 35, together with the specification, page 6. “Substantially the same rate” is defined as providing the dielectric material with an etch rate within 20% of the etch rate of the anti-reflective coating. See the specification, page 6. The etch rate selectivity results in exposing the contact pad without exposing the fuse covered with the dielectric material. See, e.g., claims 1, 15 and 35. Additional details of the claimed subject matter are provided in representative claims 1, 15 and 35 below:

1. A method for forming an integrated circuit comprising the steps of:
  - providing a semiconductor substrate;
  - forming a first conductive layer overlying the semiconductor substrate;
  - removing a portion of the first conductive layer to define a fuse and a conductive interconnect;
  - forming a first dielectric layer overlying the fuse and the conductive interconnect;
  - forming a bonding pad overlying the first dielectric layer, wherein the bonding pad comprises an anti-reflective layer overlying a second conductive layer, and wherein the bonding pad is electrically shorted to the conductive interconnect;
  - forming a second dielectric layer overlying the fuse and the bonding pad;

etching the second dielectric layer using a first etch process to form an exposed portion of the first dielectric layer and to form an exposed portion of the anti-reflective layer, wherein the exposed portion of the first dielectric layer overlies the fuse, and wherein the second conductive layer is not exposed by the first etch process; and

etching the exposed portion of the anti-reflective layer and the exposed portion of the first dielectric layer using a second etch process to leave a remaining portion of the first dielectric layer overlying the fuse and to expose a portion of the second conductive layer, the exposed portion of the anti-reflective layer having a first etch rate and the exposed portion of the first dielectric layer having a second etch rate, wherein the first etch rate and the second etch rate are substantially the same such that an etch selectivity of approximately 1:1 is achieved between the exposed portion of the anti-reflective layer and the exposed portion of the first dielectric layer.

15. A method for forming an integrated circuit comprising the steps of:

providing a semiconductor substrate;

forming a fuse overlying the semiconductor substrate;

forming a first dielectric layer overlying the fuse;

forming a bonding pad overlying the first dielectric layer, wherein the bonding pad comprises an anti-reflective layer overlying a conductive layer; and

etching a portion of the anti-reflective layer and a portion of the first dielectric layer to leave a remaining portion of the first dielectric layer overlying the fuse and to expose a portion of the conductive layer, the anti-reflective layer having a first etch rate and the first dielectric layer having a second etch rate, wherein the first etch rate and the second etch rate are substantially the same such that an etch selectivity of approximately 1:1 is achieved between the anti-reflective layer and the first dielectric layer.

35. A method for forming an integrated circuit comprising the steps of:

providing a semiconductor substrate;

forming a fuse overlying the semiconductor substrate;

forming a first dielectric layer overlying the fuse;

forming a bonding pad overlying the first dielectric layer, wherein the bonding pad comprises an anti-reflective layer overlying a conductive layer; and

etching a portion of the anti-reflective layer and a portion of the first dielectric layer to leave a remaining portion of the first dielectric layer overlying the fuse and to expose a portion of the conductive layer, the anti-reflective layer having a first etch rate and the first dielectric layer having a second etch rate, wherein the second etch rate is within 20 percent of the first etch rate such that an etch selectivity of approximately 1:1 is achieved between the anti-reflective layer and the first dielectric layer.

#### PRIOR ART

The examiner relies on the following prior art references:

Yamada et al. (Yamada)	4,984,054	Jan. 8, 1991
Chew et al. (Chew)	5,057,186	Oct. 15, 1991
Douglas	5,122,225	Jun. 16, 1992
Jolly	5,419,805	May 30, 1995
Tsukude et al. (Tsukude)	5,844,295	Dec. 1, 1998

According to the examiner (Answer, page 4), appellants' admission (allegedly admitted prior art) is in the "Background of the Invention" section set forth at pages 1 and 2 of the specification.<sup>2</sup>

#### REJECTIONS

- 1) Claims 1, 2, 4, 7-10, 12, 23-25 and 28-32 under 35 U.S.C. §103 as unpatentable over the combined teachings of Tsukude, the admitted prior art, Jolly and Yamada.
- 2) Claims 5, 6, 13, 14, 26, 27, 33 and 34 under 35 U.S.C. §103 as unpatentable over the combined teachings of Tsukude, the admitted prior art, Jolly, Yamada and Douglas.
- 3) Claims 15, 16, 18, 21, 22, 35, 36, 37, 40 and 41 under 35 U.S.C. §103 as unpatentable over the combined teachings of Tsukude, the admitted prior art and Jolly.
- 4) Claims 19, 20, 38 and 39 under 35 U.S.C. §103 as unpatentable over the combined teachings of Tsukude, the admitted prior art, Jolly and Douglas.
- 5) Claims 42 and 45 under 35 U.S.C. §103 as unpatentable over the combined teachings of Tsukude, the admitted prior art, Jolly and Chew.

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<sup>2</sup> Appellants have not referred to the subject matter in the "Background of the Invention" section of the specification as "prior art". Nor have appellants admitted in the specification that such subject matter is "prior art". We find no unequivocal admission on the part of appellants in the specification. In re Nomiya, 509 F.2d 566, 571, 184 U.S.P.Q. 603, 611-12 (CCPA 1975) .

- 6) Claims 43, 44, 46 and 47 under 35 U.S.C. §103 as unpatentable over the combined teachings of Tsukude, the admitted prior art, Jolly, Yamada and Chew.

### OPINION

We have carefully reviewed the claims, specification and prior art, including the arguments presented by the examiner and appellants in support of their respective positions. This review has led us to conclude that the examiner has not provided sufficient evidence to establish a *prima facie* case of unpatentability. Accordingly, we reverse each of the examiner's section 103 rejections.

Appellants contend that the prior art references do not teach or suggest, *inter alia*, the claimed etch selectivity ratio of the dielectric material to the anti-reflecting coating of approximately 1:1 (1.2:1 to 0.8:1)<sup>3</sup>. Thus, the dispositive question is whether it would have been *prima facie* obvious to employ the claimed etch ratio in the process of Tsukude. On this record, we answer this question in the negative.

As acknowledged by the examiner, Tsukude and the allegedly admitted prior art do not describe the employment of the claimed etch ratio in the fabrication of their semiconductor devices. Although the examiner relies on Jolly to show the claimed etch ratio, it only teaches an etch ratio of approximately four times greater than that claimed.<sup>4</sup> When, as here, the prior art references would have suggested a range of etch ratios outside the one claimed, the determination of optimum values thereof would not have led one of ordinary skill in the art to the claimed subject matter. See In re Sebek, 465 F.2d 904, 907, 175 USPQ 93, 95 (CCPA 1972)

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<sup>3</sup> The etch rate of dielectric material is within 20% of the etch rate of the anti-reflecting coating.

<sup>4</sup> We also note that the Jolly reference teaches a device materially different from those described in Tsukude and the allegedly admitted prior art.

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(“Where, as here, the prior art disclosure suggests the outer limits of the range of suitable values, and the optimum resides within that range, and where there are indications elsewhere that in fact the optimum should be sought within that range, the determination of optimum values outside that range may not be obvious.”).

CONCLUSION

For the reasons set forth above and in the Brief, we agree with appellants that the examiner has not presented a *prima facie* case of unpatentability. Accordingly, the decision of the examiner is reversed.

REVERSED

CHUNG K. PAK	)	
Administrative Patent Judge	)	
	)	
	)	BOARD OF PATENT
THOMAS WALTZ	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
JEFFREY SMITH	)	
Administrative Patent Judge	)	

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