

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DOMINIQUE SAVIGNAC, FRANK WEBER and NORBERT WIRTH

Appeal No. 2001-2459
Application No. 09/277,281

ON BRIEF

Before BARRETT, RUGGIERO and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1, 4-7 and 10-12. Claims 2, 3, 8 and 9 have been cancelled.

We reverse.

BACKGROUND

Appellants' invention is directed to a circuit configuration for identifying contact failure during the testing of integrated circuits before being incorporated in a circuit board. If, for example, contact is not made with all the active "low" pins of an

integrated circuit which are connected to external pads during the testing, the circuits behave as if they were activated and are assessed as "pass" (specification, page 2). In order to cause only those circuits that have been checked for their functionality be assessed as "good" or "pass," Appellants provide for a pull-up or pull-down device for holding the corresponding pad at a high or low potential (specification, page 4). Thus, if contact is not made with a pin during testing, activating a circuit section connected to that pin can be avoided (id.).

Independent claim 1 is reproduced as follows:

1. An integrated circuit configuration for identifying contact faults during testing of the integrated circuit configuration, comprising:

a semiconductor body;

pads disposed on said semiconductor body;

input buffers connected to said pads and defining a connection node between each respective pad and a respective input buffer;

a housing protecting said semiconductor body;

a multiplicity of pins protruding from said housing and connected to said pads; and

a pull-up device connected to said connection node between said respective pad and said respective input buffer, said pull-up device holding said respective pad at a high potential by impressing a holding current if contact has not been made with a pin associated with said respective pad during testing resulting in avoiding activating a circuit

Appeal No. 2001-2459
Application No. 09/277,281

section connected to said pin associated with said respective pad, said pull-up device having a P-channel MOS transistor with a gate and connected between said connection node and a high potential, said gate receiving a voltage for controlling said P-channel MOS transistor, said pull-up device having a further P-channel MOS transistor with a further gate and connected between said connection node and the high potential, said further gate receiving a low potential.

The following reference is relied on by the Examiner:

| | | |
|----------|-----------|---------------------------------------|
| Intrater | 5,818,251 | Oct. 6, 1998 (filed Jun. 11, 1996) |
|----------|-----------|---------------------------------------|

Claims 1, 4-7 and 10-12 stand rejected under 35 U.S.C.

§ 102(e) as being anticipated by Intrater.

Rather than reiterate the viewpoints of the Examiner and Appellants, we make reference to the answer (Paper No. 15, mailed April 18, 2001) for the Examiner's complete reasoning and the brief (Paper No. 14, filed February 26, 2001) for Appellants' arguments thereagainst.

OPINION

Appellants argue that Intrater cannot anticipate the claimed subject matter as the reference is merely directed to applying a high voltage and a low voltage to each conductive trace in order to test for a proper connection (brief, page 12). Appellants further state that the circuit connections of Intrater are directly tested whereas the claimed subject matter relates to

Appeal No. 2001-2459
Application No. 09/277,281

measuring the output performance of a circuit and what Intrater describes as "functional tester" (id.). Additionally, Appellants assert that the reference teaches neither a pull-up device holding the pad at a high potential, nor two MOS transistors receiving high and low potentials respectively (id.).

In response to Appellants' arguments, the Examiner relies on Figure 1 of Intrater and points out that the claimed pull-up device is shown as the MOS FET transistor 46 whereas the second MOS transistor is disclosed as the NPN Bipolar Junction Transistor (BJT) MOS 30 (answer, page 6). Additionally, the Examiner asserts that the gate of the MOSFET transistor 46 "receives a voltage (V_{TEST}) for controlling the P-channel" and a second MOS transistor pull-down device is provided with a "holding current (V_{LOAD})" (id.).

A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. See Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999); In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994). Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well

Appeal No. 2001-2459
Application No. 09/277,281

as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys. Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Upon a review of Intrater, we agree with Appellants that the reference fails to teach a pull-up device including two MOS transistors for holding the pad at a high potential. The apparatus for testing the pin connections of Intrater tests the connection between internal circuits of an integrated circuit, a plurality of I/O pins, and conductive traces on a circuit board by coupling a voltage source to the pins and comparing the voltage level on the conductive traces with predetermined levels (col. 3, lines 21-35). This arrangement differs from the claimed "said pull-up device holding said respective pad at a high potential by impressing a holding current if contact has not been made with a pin" since the value of the voltage on the conductive trace of Intrater determines if connection is made rather than preventing the activation of a disconnected pin.

With respect to the Examiner's characterization of the npn bipolar junction transistor 30 of Intrater as a MOS transistor, we recognize that the claims require two P-channel MOS transistors in the pull-up device of claim 1 and two N-channel

MOS transistors in the pull-down device of claim 7. The fact that the channel conductivity of the MOS transistors is specified as either P or N, clearly indicates that the transistors are field effect transistors and a bipolar junction transistor (BJT) cannot qualify as a P or N-channel MOS transistor.

Additionally, we observe that the examiner appears to have corresponded active pull-up resistance 42 in figure 1 of Intrater, which may alternatively consist of field effect transistor 46, to the pull-up device of independent claim 1 (answer, page 4). The examiner further corresponds transistor 30 in Figure 1 of Intrater as the pull-down device of independent claim 7 (answer, page 5). However, the Examiner, in the "Response to Argument" section, points out that nowhere in the claims are two MOS transistors recited and Appellants merely recite a pull-up transistor in claim 1 or a pull-down transistor in claim 7 (answer, page 6). In these arguments, the Examiner ignores the recited limitations of both claims 1 and 7 requiring two MOS transistors in each of the pull-up or the pull-down devices, respectively. Thus, transistor 30 of Intrater is not only a bipolar transistor, and NOT a MOS field effect transistor, but even as a switch, functions differently from the claimed second MOS transistor in either the pull-up device of claim 1 or

Appeal No. 2001-2459
Application No. 09/277,281

the pull-down device of claim 7. Transistor 30, in fact, is external to integrated circuit 6 and a part of test circuit 2 that checks the connection between I/O pin 4 of integrated circuit 6 and conductive traces 8 on a printed circuit board (PCB) (col. 5, lines 58-62). Contrary to the Examiner's assertion (answer, page 6), since only the MOS transistor 46 of Intrater is determined to be a pull-up device connected between pin 4 and input/output buffer 40 (col. 7, lines 33-35), the only other transistor connected to pin 4, which is bipolar transistor 30 or a switch in external test circuit 2, cannot act as a second MOS transistor in the pull-up device. The subject matter of claims 1 and 7 would not, therefore, have been prima facie anticipated by Intrater. Accordingly, we do not sustain the rejection of claims 1, 4-7 and 10-12.

Appeal No. 2001-2459
Application No. 09/277,281

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1, 4-7 and 10-12 under 35 U.S.C. § 102 is reversed.

REVERSED

| | | |
|-----------------------------|---|-----------------|
| LEE E. BARRETT |) | |
| Administrative Patent Judge |) | |
| |) | |
| |) | |
| |) | |
| JOSEPH F. RUGGIERO |) | BOARD OF PATENT |
| Administrative Patent Judge |) | APPEALS AND |
| |) | INTERFERENCES |
| |) | |
| |) | |
| MAHSHID D. SAADAT |) | |
| Administrative Patent Judge |) | |

MDS/ki

Appeal No. 2001-2459
Application No. 09/277,281

Lerner and Greenberg, P.A
Post Office Box 2480
Hollywood, FL 33022-2480