

The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 30

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DENNIS E. GATES and SCOTT E. GREENFIELD

Appeal No. 2001-2351
Application No. 08/772,443

ON BRIEF

Before URYNOWICZ, FLEMING and BARRY, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

Decision on Appeal

This appeal is from the final rejection of claims 1, 3, 4, 9, 11, 12, 17-26 and 31-34. In the answer at page 7, lines 16-18, the examiner has withdrawn the rejection of claims 24 and 25, and has indicated that those claims are allowable.

The invention pertains to a controller. Claim 1 is illustrative and reads as follows:

Appellants' Invention

The invention of Figure 1 provides a mechanism by which data transfers from a peripheral interface 120 of a disk array to a data buffer 114 are snooped to determine if the starting address of a data transfer matches an entry in a list of starting addresses stored in host interface control 112. If snooping circuit 422 (Figure 4) of host interface control 112 detects a match between an actual data transfer starting address and a starting address in a list of data transfers in a queue, the snooping circuit signals a buffer interface control unit 404 to initiate transfer of the data on a buffer data bus 116 into a buffer bus interface unit 400. By doing so, data may be obtained for a host interface directly from a peripheral interface control 110 via the buffer data bus 116 without first storing the data in the data buffer 114, and subsequently transferring the data via a host interface control 112 to the host interface and, ultimately, to the host system (Figure 1). By virtue of the present invention, a current data transfer from interface control 110 may be simultaneously received by both the data buffer and the host system.

The Prior Art

In Figure 3 of Parks, a caching disk controller 304 is provided which includes a bus bridge 320 that forms an interface between a memory 324 of the disk controller and a host computer 302, 303. The caching disk controller 304 further includes SCSI processor 328, 330 for controlling the transfer of data from a SCSI disk drive 306 to the memory 324 via a local bus 326. A zero latency DMA controller 408 (Figure 4) embodied within the bus bridge snoops the local bus 326 as data is being transferred from the SCSI disk drive to the memory 324, and thereby allows the data to be sequentially latched within a data FIFO 504 (Figure 5) of the bus bridge concurrently with its transfer into the memory. As a result, the requested data may be provided from the bus bridge to the host computer with reduced delay, while the data continues to be stored within the memory 324 to accommodate high hit rates during subsequent transfers.

The Rejection under 35 U.S.C. § 102(e)

Independent Claims 1, 4, 9, 20 and 31

Appellants argue that local memory 324 in Figure 3 of Parks is a cache memory, which is not the same as a data buffer. Purportedly, a buffer is not interchangeable with a cache because the functionality of the two devices are different. It is urged

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that the purpose and functionality of a cache is to accelerate the speed of an activity by storing instructions/data that are likely to be required by a processor multiple times. In contrast, appellants contend a buffer is simply a temporary storage for slowing down the I/O from one device to match the I/O speed of another device.

Appellants urge that even if it were true that a cache and a buffer are equivalents, the reference does not anticipate the disclosed invention because it requires data to be passed through a buffer, i.e. data FIFO 504.

The examiner's position with respect to appellants' first argument is that several publications were cited at pages 3-5 of the final rejection to establish that a buffer is equivalent to a cache memory. With respect to the second of appellants' arguments, the examiner asserts to the effect that the data in Parks transfers from the bus 326 to the host 303 without requiring transfer of the data "using" (claim 1) the local memory (buffer) 324.

We will not sustain the rejection of claims 1, 4, 9, 20 and 31 as anticipated by Parks. We do not agree with the examiner's position to the effect that the local memory 324 of Parks is a buffer. Memory 324 of Parks is disclosed as a cache memory, not

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as a buffer, and at page 2, line 27 to page 3, line 7, appellants disclose that their invention relates to non-cached disk read operations and apparatus. The written description can provide guidance as to the intended meaning of the claims, thereby dictating the manner in which the claims are to be construed, even if the guidance is not provided in explicit definitional format. SciMed Life Systems v. Advanced Cardiovascular Systems, 242 F.3d 1337, 1344, 58 USPQ2d 1059, 1065 (Fed. Cir. 2001). Accordingly, appellants' claimed buffer is not met by Parks' cache memory, and the buffer of the claims is not broad enough to encompass a cache memory.

Although we will not sustain the rejection of claims 1, 4, 9, 20 and 31, we agree with the examiner that transfer of data from the bus to the host without requiring transfer of the data using the data buffer is taught by Parks. Assuming for purposes of argument only that local memory 324 of Parks is a buffer, Parks transfers data from bus 326 to the host 303 without requiring transfer of the data using data buffer 324 because on readout, the data from SCSI devices 306 proceeds through processors 328 or 330, bus 326, snooping bus bridge 320, and bus 306 without using buffer 324.

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The Rejection under 35 U.S.C. § 102(e)

Independent Claim 23

We will not sustain this rejection because Parks' local memory 324 is not a data buffer, and because we agree with appellants that Parks does not teach a "list of requested data transfers".

At page 7 of the answer, the examiner avers that, in his Description of the Relevant Art, Parks teaches a list of requested data transfers at column 1, line 50, to column 2, line 5. This text in pertinent part teaches at column 1, lines 59-67 that,

a sector read request is transmitted by the host processor 102 and is written into the host interface register file 206 of bus bridge 120. Bus bridge 120 responsively asserts an interrupt to alert local processor 122 of the pending request. Local processor 122 subsequently reads the pending request within the host register file 206...(emphasis added).

This is a teaching that there is one request for data in file 206; there is nothing in the text to indicate that there is a list of requested data in the file.

The Rejection under 35 U.S.C. § 102(e)

Independent Claims 17, 19 and 26

We will not sustain the rejection of these claims because Parks' local memory is not a buffer, and because we agree with

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appellants that Parks does not teach that the current data transfer is simultaneously received by the data buffer and the host system. At page 8 of the answer, the examiner argues to the effect that the claimed feature is met by Parks because the data received from the peripheral devices is sent to local memory 324 in Figure 3 and FIFO 504 in Figure 5 at the same time.

Although the examiner is correct in his characterization of Parks' teaching, this teaching does not meet the claimed subject matter. The claims require that the data transfer is simultaneously received by the data buffer and the host system. In Parks, the data transfer is simultaneously received at local memory 324 and the FIFO 504 of the snooping bus bridge 320. See column 7, lines 48-51. Even if it is assumed that the data buffer of the claims is met by Parks' local memory 324, the FIFO 504 is not a part of the host system. The host system of Parks comprises processor 302 and the data in FIFO 504 is subsequently transferred to the processor.

The Rejection under 35 U.S.C. § 102(e)

Claims 3, 11, 12, 18, 21, 22 and 32-34

Whereas we will not sustain the rejection of any independent claim, we will not sustain the rejection of dependent claims 3, 11, 12, 18, 21, 22 and 32-34 as anticipated by Parks.

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Summary

In summary, the rejection of claims 1, 3, 4, 9, 11, 12, 17-23, 26 and 31-34 will not be sustained.

REVERSED

STANLEY M. URYNOWICZ JR.)	
Administrative Patent Judge)	
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MICHAEL R. FLEMING)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
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