

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HASHEM FARROKH, KALAVAI J. RAGHUNATH and
SUBRAMANIAN NAGANATHAN

Appeal No. 2001-2125
Application No. 08/906,537

ON BRIEF

Before FLEMING, RUGGIERO, and BLANKENSHIP, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1-3 and 5-18, which are all of the claims pending in the present application. Claim 4 has been canceled.

The disclosed invention relates to the cooperative combination of a computer-implemented multiplier and accumulator. One of the input terms to the multiplier is encoded with a partial product reducing methodology such as Booth encoding. More particularly, a

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selected one of the "round" bits introduced by the Booth encoding is processed at an otherwise unused input terminal of the accumulator without affecting the overall result of the multiplier/accumulator operation. According to Appellants (specification, page 12), the removal of the selected "round" bit from the partial product adders of the multiplier permits an elimination of a full adder stage from the multiplier.

Claim 1 is illustrative of the invention and reads as follows:

1. A method for cooperatively combining a computer-implemented multiplier and an accumulator established to receive an output of said multiplier comprising the steps of:

causing an input term of said multiplier to be coded according to an algorithm for reducing a number of partial products generated by operation of said multiplier;

configuring adder stages of said multiplier for summing said partial products so that all partial product bits except for at least one round bit are processed in a set of adders comprising said adder stages;

causing said at least one round bit to be processed by said accumulator; and

causing an output of said multiplier to be provided as an input to said accumulator.

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The Examiner relies on the following prior art:

Essig et al. (Essig)	4,646,257	Feb. 24, 1987
Ozaki	5,303,178	Apr. 12, 1994
Taborn et al. (Taborn)	5,550,767	Aug. 27, 1996
De Angel	5,787,029	Jul. 28, 1998

(filed Jan. 10, 1997)

Claims 1-3 and 5-18, all of the appealed claims, stand finally rejected under 35 U.S.C. § 103(a). As evidence of obviousness, the Examiner offers Taborn in view of De Angel with respect to claims 1, 3, 5-12, 17, and 18, separately adds Ozaki to the basic combination with respect to claims 2 and 13, and separately adds Essig to the basic combination with respect to claims 14-16.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief (Paper No. 19) and Answer (Paper No. 20) for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner, the arguments in support of the rejection and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Brief along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

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It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1-3 and 5-18. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed.

Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

With respect to independent claims 1, 12, 17, and 18, the Examiner, as the basis for the obviousness rejection, proposes to modify the disclosed circuitry of Taborn which describes, as illustrated in Figure 1, a cooperative combination of a multiplier (20) and an accumulator (23 and 30). As recognized by the Examiner (Answer, page 4), Taborn ". . . does not specifically disclose the structure of the multiplier and thus does not teach a coding of the multiplier, a plurality of adder stages and an adding of round bits as claimed." To address these deficiencies, the Examiner turns to De Angel which discloses multiplier circuitry utilizing Booth encoding in which the "rounding bits" are not added in the various adder stages but, rather, are processed by the following adder 30. In the Examiner's analysis (id.), the skilled artisan, motivated by power saving advantages, would have found it obvious to provide Taborn with a multiplier as taught by De Angel, with the combined teachings resulting ". . . in a combination of a multiplier and an accumulator which does not add the 'rounding bit' in the partial product adder stages but in the accumulator as claimed."

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In response to the obviousness rejection, Appellants assert several arguments in support of their contention that the Examiner has failed to establish a prima facie case of obviousness. In particular, Appellants assert (Brief, pages 8-10) that no clear motivation for combining Taborn with De Angel has been provided by the Examiner, and, even if combined, the ensuing structure would not result in the particular combination as claimed.

After reviewing the arguments of record from both Appellants and the Examiner, we are in general agreement with Appellants' position as stated in the Brief. In particular, our interpretation of the disclosure of De Angel coincides with that of Appellants, i.e., the adder stage 30, which the Examiner asserts is adding "round bits" A1-A7, is merely an end-stage adder for the multiplier itself. Given this disclosure of De Angel, it is not apparent as to how and in what manner Taborn would be modified to produce the structure as claimed in which "round bits" are provided as inputs to the accumulator part of the multiply/accumulator cooperative combination.

We recognize that the Examiner, in the "Response to Argument" portion of the Answer at page 6, suggests the well-known aspects of modifying a multiplier to form a multiplier/accumulator by introducing a 3-2 carry save adder between a multiplier array and a

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full adder. Initially, we would point out that the Examiner has provided no evidence to support such an assertion. "[T]he Board cannot simply reach conclusions based on its own understanding or experience - or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings." In re Zurko, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). The court has also recently expanded their reasoning on this topic in In re Thrift, 298 F. 3d 1357, 1363, 63 USPQ2d 2002, 2008 (Fed. Cir. 2002).

We are further of the opinion that, even assuming arguendo that the Examiner's supposition was supported by a proper evidentiary showing, there is no further showing that substituting the multiplier array of De Angel for the multiplier 20 of Taborn would necessarily result in a structure in which a "round bit" would be introduced and processed at the accumulator stage of the multiply/accumulator as claimed. Although the Examiner suggests (Answer, pages 6 and 7) that the structure of Taborn modified with De Angel would result in the adding of "round bits" in the accumulator, we find such an assertion to be based solely on unwarranted speculation. In order for us to sustain the Examiner's rejection, we would need to resort to impermissible speculation or

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unfounded assumptions or rationales to supply deficiencies in the factual basis of the rejection before us. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), rehearing denied, 390 U.S. 1000 (1968).

In view of the above discussion, since the Examiner has not established a prima facie case of obviousness, the 35 U.S.C. § 103(a) rejection of independent claims 1, 12, 17, and 18, as well as claims 3, and 5-11 dependent thereon, based on the combination of Taborn and De Angel, is not sustained.

We also do not sustain the Examiner's obviousness rejection of claims 2 and 13 in which Ozaki is added to Taborn and De Angel, nor the obviousness rejection of claims 14-16 in which Essig is added to Taborn and De Angel. We have reviewed the Ozaki and Essig references, added by the Examiner as providing a teaching of sign bit changing and adder stage counting, respectively. We find nothing, however, in either of these references that would overcome the innate deficiencies of Taborn and De Angel discussed supra.

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In summary, we have not sustained the Examiner's 35 U.S.C. § 103(a) rejection of any of the claims on appeal. Accordingly, the decision of the Examiner rejecting claims 1-3 and 5-18 is reversed.

REVERSED

MICHAEL R. FLEMING)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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HOWARD B. BLANKENSHIP)	
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