

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANDREW H. SIMON and CYPRIAN E. UZOH

Appeal No. 2001-1118
Application 09/262,690¹

ON BRIEF

Before LEE, LANE and MEDLEY, Administrative Patent Judges.

MEDLEY, Administrative Patent Judge.

DECISION ON APPEAL

A. Introduction

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 11-27. For the reasons that follow, the rejection is reversed.

Summary of the involved technology

Semiconductor chips contain electrical devices that are interconnected through conductive wires. To conserve "space" on a semiconductor chip, multiple levels of conductive lines are desirable. The multiple levels of conductive lines are vertically spaced apart, separated

¹ Application for patent filed 4 March 1999.

by insulating layers. Electrical connection can be made between the different levels of conductive lines by means of vias which extend through the insulating layers to the conductive lines. The vias are filled with metal to form a stud. Prior to filling the via with a conductive material, a liner layer is deposited on the side walls and bottom of the via, such as to form a barrier in between the conductive metal deposited in the via and the insulative layers.

According to the involved application, the material used for the liner layer tends to be resistive and because of its presence on the bottom of the via adds to the overall resistance of the conductive stud. Such added resistance is not desirable, since it leads to slower propagation of electrical signals.

The claimed invention attempts to solve the problem of the added resistance by removing the bottom layer of the liner. The applicants have claimed a semiconductor article having a material with a via. A first layer is deposited in the via and a second layer is deposited on the first layer. During the sputtering process of depositing the second layer on the first layer, the first layer deposited on the bottom of the via is “substantially removed,” while the first layer deposited on the sidewalls remains on the sidewalls.

B. Findings of Fact

1. The applicants state that the real party in interest is International Business Machines Corporation. (Brief at 2).
2. The application on appeal contains claims 11-27.
3. Claims 1-10 have been cancelled.
4. Claims 11, 13, 14, 16 and 17 have been rejected as being anticipated under 35

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U.S.C. § 102(b) by Chakravorty et al. (Chakravorty), U.S. Patent 5,436,504, issued 25 July 1995, based on application 09/064,794, filed 19 May 1993.

5. Claim 12 has been rejected as being unpatentable under 35 U.S.C. § 103 over Chakravorty in view of Nakajima et al. (Nakajima), U.S. Patent 5,444,302, issued 22 August 1995, based on application 09/168,506, filed 22 December 1993.

6. Claims 15 and 18-27 have been rejected as being unpatentable under 35 U.S.C. § 103 over Chakravorty in view of Hoshino, U.S. Patent 4,985,750, issued 15 January 1991, based on application 07/097,738, filed 17 September 1987.

7. The independent claims are reproduced as follows:

11. A semiconductor article comprising:

- a. a material having a via;
- b. a first layer deposited in the via, the first layer lining the via;
- c. a second layer deposited on the first layer, the second layer is deposited using Rf biased sputter deposition; wherein the first layer deposited on the bottom of the via is substantially removed during the Rf biased sputter deposition of the second layer but substantially all of the first layer deposited on the sidewalls of the via during the Rf biased sputter deposition of the second layer is unaffected.

18. A semiconductor article comprising:

- a. a material having a via;
- b. a first layer deposited in the via, the first layer lining the via;
- c. a second liner layer deposited on the first liner layer, the second layer is deposited using Rf biased sputter deposition; wherein the first layer deposited on the bottom of the via is substantially removed during the Rf biased sputter deposition of the second layer

but substantially all of the first layer deposited on the sidewalls of the via during the Rf biased sputter deposition of the second layer is unaffected and wherein the second liner layer is also substantially removed from the bottom of the via during the sputter deposition.

23. A semiconductor article comprising:

a. a material having a via;

b. a first layer deposited in the via, the first layer lining the via;

c. a second liner layer deposited on the first liner layer, the second layer is deposited using Rf biased sputter deposition; wherein the first layer deposited on the bottom of the via is substantially removed during the Rf biased sputter deposition of the second layer but substantially all of the first layer deposited on the sidewalls of the via during the Rf biased sputter deposition of the second layer is unaffected.

8. The applicants' specification defines "substantially removed" as follows:

By "substantially removed" it is meant that the amount of first deposited material remaining on the bottom of the via, 100, after the sputter deposition is insufficient to significantly effect the electrical and capacitive potential of the final structure. (Application at 12, lines 1-5).

The Chakravorty reference

9. Chakravorty discloses an interconnect structure with a layer of tantalum metal and tantalum oxide in between the conductor and the insulator in the interconnect structure. (Col. 3, lines 1-4). The tantalum/tantalum oxide layer is patterned to expose the underlying electroplating seed layers, while maintaining electrical contact between the electroplating seed layers and the edges of the substrate through the tantalum layer. (Col. 3, lines 51-55).

Chakravorty explains that "[t]he underlying tantalum layer will ensure good electrical interconnection of all of the individual plating seed layers" (col. 6, lines 14-16) and that the

etching of the tantalum/tantalum oxide layer is accomplished by retaining a sufficient overlap of the tantalum/tantalum oxide layer over the seed layer to ensure good electrical contact between the tantalum and the plating seed layer. The overlap is described as being about 2-3 microns. (Col. 6, lines 35-41).

B. Discussion

The applicants in their brief indicate that claims 11-27 stand or fall together. (Brief at 3).

We reverse the rejections of claims 11-27 as follows. A reversal of the rejection on appeal of claims 11-27 should not be construed as an affirmative indication that the applicants' claims are patentable over prior art. We address only the positions and rationale as set forth by the examiner and on which the examiner's rejection of the claims on appeal is based.

The examiner finally rejected: (1) independent claim 11 as being anticipated under 35 U.S.C. § 102(b) by Chakravorty, and (2) independent claims 18 and 23 as being unpatentable under 35 U.S.C. § 103 over Chakravorty in view of Hoshino. In both the anticipation and the obviousness rejections, the examiner relies on Chakravorty to teach a first liner layer that is "substantially removed" as recited in applicants' independent claims 11, 18 and 23.

The issue, as presented, is whether Chakravorty teaches a first liner layer that is deposited on the bottom of a via that is "substantially removed." Thus, if the examiner has failed to sufficiently establish that Chakravorty teaches a first liner layer that is "substantially removed," the rejections of all of the claims 11-26 must be reversed.

Applicants argue that "substantially removed" has a specific meaning as defined in its specification. The term "substantially removed" is specifically defined in the specification to

mean that any liner material remaining on the bottom of the via is insufficient to significantly effect the electrical and capacitive potential of the final structure (ff² 8). The examiner apparently does not disagree that the term “substantially removed” should be interpreted with the specific meaning set forth in the applicants’ specification, rather the examiner states that “the appellant has failed to discuss or present evidence as to what electrical or capacitive potential effect would an overlap of 2-3 microns on a seed layer close to the bottom of the via would have in terms of functionality.” (Answer at 9; Supplemental Answer³ at 9).

The applicants have specifically defined “substantially removed.” When an applicant states the meaning that the claim terms are intended to have, the claims are examined with that meaning, in order to achieve a complete exploration of the applicant’s invention and its relation to the prior art. *In re Zletz*, 898 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Here, the applicants have selected to specifically set forth a definition for “substantially removed” to mean that any material remaining on the bottom of the via is insufficient to significantly effect the electrical and capacitive potential of the final structure⁴.

Although Chakravorty teaches removing a portion of the first liner layer from the bottom of the via, Chakravorty describes leaving enough of the first layer to “ensure good electrical contact” between the first layer and the underlying seed layer. Contrary to the examiner’s

² Finding of fact.

³ The Examiner’s Supplemental Answer repeats those arguments made in the Examiner’s Answer.

⁴ We understand “final structure” to refer to the final structure of the via.

suggestion, the applicants need not present additional evidence as to the electrical or capacitive potential of the overlap. The Examiner initially bears the burden of establishing a prima facie case of anticipation or obviousness based upon the prior art. Here, the examiner has failed to sufficiently demonstrate that Chakravorty meets the “substantially removed” feature as defined in the applicants’ specification, by explaining why the first liner layer overlap taught in Chakravorty is insufficient to significantly effect the electrical and capacitive potential of the final via structure. Based on the record before us, Chakravorty teaches an overlap that is significant to ensure good electrical contact with the underlying seed layer. As the seed layer is apparently part of the final structure of the via, such electrical contact between the seed layer and the liner layer would significantly effect the electrical and capacitive potential of the final via structure. The examiner fails to provide a contrary explanation, and therefore we cannot sustain the rejection of claims 11-27.

Independent claims 18 and 23 and dependent claims 15, 19-22 and 24-27 were rejected based on the combination of Chakravorty and Hoshino. The examiner relies on Hoshino to teach a specific TaN/Ta liner layer, and not to teach the “substantially removed” feature of the first liner layer. Consequently, as applied by the examiner, Hoshino does not make up for the deficiencies of Chakravorty.

For dependent claim 12, the examiner relies on Nakajima to teach a first layer of semiconductor material and not to teach the “substantially removed” feature of the first liner layer. As applied by the examiner, Nakajima does not make up for the deficiencies of Chakravorty.

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For the above reasons, the rejection of (1) claims 11, 13, 14, 16 and 17 as being anticipated under 35 U.S.C. § 102(b) by Chakravorty, (2) claim 12 as being unpatentable under 35 U.S.C. § 103 over Chakravorty in view of Nakajima, and (3) claims 15 and 18-27 as being unpatentable under 35 U.S.C. § 103 over Chakravorty in view of Hoshino cannot be sustained.

The examiner's rejection of claims 11-27 is reversed.

REVERSED

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JAMESON LEE)	
Administrative Patent Judge)	
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SALLY GARDNER LANE)	INTERFERENCES
Administrative Patent Judge)	
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SALLY C. MEDLEY)	
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