

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAUL R. BESSER, DARRELL M. ERB,
and SERGEY LOPATIN

Appeal No. 2001-1090
Application No. 09/477,821

ON BRIEF

Before HAIRSTON, JERRY SMITH, and BLANKENSHIP, Administrative Patent Judges.
HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 20.

The disclosed invention relates to a method of manufacturing an electrical device in which in-laid unalloyed copper in the upper surface of a dielectric layer is subjected to an alloying process. Prior to the alloying process, the unalloyed copper is co-planar with the upper surface of the dielectric layer.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A method of manufacturing an electrical device, which method comprises the sequential steps of:

(a) providing a substrate including at least one metal feature in-laid in the upper, exposed surface of a layer of dielectric material overlying at least a portion of said substrate, the at least one metal feature including an upper, exposed surface substantially co-planar with said upper surface of said layer of dielectric material;

(b) selectively depositing at least one layer comprising at least one alloying element for said metal feature on said exposed, upper surface of said at least one metal feature; and

(c) annealing to substantially uniformly diffuse at least a predetermined minimum amount of said at least one alloying element from said at least one layer comprising said at least one alloying element into said at least one metal feature for at least a predetermined minimum depth below the upper surface thereof, whereby electromigration of metal of said at least one metal feature is minimized or substantially prevented.

The references relied on by the examiner are:

Chiu et al. (Chiu)	4,335,506	June 22, 1982
Chow et al. (Chow)	4,789,648	Dec. 6, 1988
Kondo et al. (Kondo)	6,001,736	Dec. 14, 1999
Nogami et al. (Nogami)	6,022,808	Feb. 8, 2000
		(filed Mar. 16, 1998)

Claims 1 through 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nogami in view of Chow, Chiu and Kondo.

Reference is made to the briefs (paper numbers 10 and 12) and the answer (paper number 11) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1 through 20.

As the title indicates, Nogami recognizes the problem of copper (Cu) electromigration¹ from Cu interconnects into surrounding device structures. Nogami's method of semiconductor manufacture starts with the deposit of undoped Cu 13 into hole 12 in dielectric layer 10 (Figure 1). The undoped Cu 13 is not "co-planar with" the upper surface of the dielectric layer 10. "A layer of doped Cu 14 is then sputter deposited on the undoped Cu layer 13" (column 5, lines 64 and 65). An annealing step is then performed to diffuse dopant element atoms from the doped Cu layer 14 into the undoped Cu layer 13 to thereby transform the undoped Cu layer 13 into a doped Cu layer 20 (Figure 2; column 5, line 66 through column 6, line 2). According to Nogami (column 6, lines 2 through 5), "[b]y annealing to diffuse dopant element atoms from doped Cu layer 14 into undoped Cu layer 13, the electromigration resistance of Cu layer 20 filling via hole 12 is significantly improved." Thereafter, a chemical-mechanical polishing (CMP) step is performed to make the surface of electromigration resistant Cu via 20 "co-planar with" the upper surface of dielectric layer 10 (Figure 3; column 6, lines 5 through 8).

Appellants and the examiner all recognize that the steps of the claimed invention require making the in-laid Cu and the surface of the dielectric layer "co-planar with" each other prior to the

¹ The same problem is addressed by appellants (specification, page 4, lines 7 through 9).

annealing step of the in-laid Cu, whereas Nogami clearly discloses a step of making the in-laid Cu “co-planar with” the surface of the dielectric layer subsequent to the annealing step of the in-laid Cu (brief, pages 13, 14 and 16; answer, page 4).

The secondary reference² to Chow was cited by the examiner because it teaches “a planarization step following the deposition of a metal into a damascene (Fig. 5 & 6),” and the secondary reference to Chiu was cited by the examiner because it teaches “a process wherein a conductive layer may be formed and wherein an alloying material may be selectively deposited or patterned over the conductive layer before the annealing step (col. 1, lines 5-20)” (answer, page 4). Based upon the teachings of these references, the examiner opines that “[i]t would have been obvious to one having ordinary skill in the specific art to pattern the metal before the alloying step and to selectively deposit the alloying material, since the applicant has [sic, applicants have] not disclosed that patterning the metal before the alloying step solves any stated problem or is for any particular purpose and it appears that he [sic, the] invention would perform equally well with the alloying step being performed first.”

As indicated supra, appellants have recognized and solved the same problem recognized and solved by Nogami, albeit via differently ordered process steps. Notwithstanding Nogami’s alloying before planarization steps, the teachings of Nogami, or any other evidence of record presented by way of either Chow or Chiu, do not offer proof that it would have been obvious to one of ordinary

² We assume that the secondary reference to Kondo was cited for its relevance to the “hydrogen plasma” in dependent claim 13.

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skill in the art to reverse the order of the process steps disclosed by Nogami to meet the claimed order of process steps. Appellants argue (reply brief, page 4) that the only evidence of record of such a switch of process steps is their disclosed and claimed invention, and that such teachings are not available to the examiner in an obviousness determination. We agree. Thus, the obviousness rejection of claims 1 through 20 is reversed because “the combination of references as postulated by the Examiner does not and cannot remedy the inherent deficiency of the primary reference and yield the claimed invention in that they do not disclose or even remotely suggest performing planarization of the blanket metallization layer prior rather than subsequent to deposition (selective) of the alloying element layer(s)” (brief, page 16).

DECISION

The decision of the examiner rejecting claims 1 through 20 under 35 U.S.C. § 103(a) is reversed.

REVERSED

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KENNETH W. HAIRSTON
Administrative Patent Judge

JERRY SMITH
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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