The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DALE E. GULICK

Appeal No. 2001-0594
Application No. 08/929,153

ON BRIEF

Before THOMAS, KRASS and GROSS, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-19, 21-23, 25 and 26.

The invention is directed to power management in computer systems. More specifically, logic functions are partitioned across two chips interconnected by a serial bus. The bus is placed in a power savings mode and is used to communicate the

existence of a wake-up event from one chip of the partition to another.

Representative independent claim 1 is reproduced as follows:

1. A method of providing an indication to a first integrated circuit that a wake-up event has been detected by a second integrated circuit, the first and second integrated circuits being coupled by a bus having signal lines including a bus clock, a data in signal line and a data out signal line, the method comprising:

placing the bus in a reduced power consumption state wherein the signal lines, including the bus clock, are inactive;

signaling the existence of the wake-up event to the first integrated circuit by changing at least one signal line of the bus from a first voltage level to a second voltage level while the bus clock is inactive, in response to the wake-up event detected by the second integrated circuit;

changing the bus from the reduced power consumption state to a normal power consumption state in response to the one signal line being at the second voltage level, the normal power consumption state including the bus clock being active; and

operating the bus in the normal power consumption state in which the signal lines transmit information in synchronism with the bus clock.

The examiner relies on the following reference:

Walsh et al. [Walsh]	5,835,733	Nov. 10, 1998 (filed Dec. 22, 1994)

Claims 1-19, 21-23, 25 and 26 stand rejected under 35 U.S.C. 102(e) as anticipated by Walsh.

Reference is made to the brief and answer for the respective positions of appellant and the examiner.

OPINION

An anticipatory reference is one that teaches each and every claimed element and its function. RCA Corp v. Applied Digital Data Sys. Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984).

Taking independent claim 1 as exemplary, the examiner contends that Walsh discloses an indication to a first integrated circuit that a wake-up event has occurred on a second integrated circuit, with the first and second integrated circuits being coupled by a bus. Specifically, the examiner points to Figure 4, elements 102, 110, 104; to column 17, lines 1-5; and to column 29, line 55, of Walsh.

Figure 4 of Walsh shows a high bandwidth bus 104 interconnecting a docking station microprocessor unit MPU 102 and a single-chip peripheral processor unit PPU 110. The cited portion of column 17 recites that when substantial portions of PPU 110 and system 102 have been deactivated by a power management block, reactivation can be initiated by circuitry in

the power management block 920 responsive to a real-time clock circuit alarm and/or other conditions. It would appear reasonable that a reactivation responsive to a real-time clock may be considered a "wake-up event."

The examiner further contends, referring to column 14, lines 64-66, and column 27, line 66 to column 28, line 2, of Walsh, that the reference teaches the placement of the bus in a reduced power consumption state. The cited portion of column 14 refers to a "bus-quieting" mode for reducing system power consumption by toggling data/address bus 104 only on bus transfers. The cited portion of column 27 to column 28 refers to the state transition diagram of Figure 23 depicting six states, "READY (0,0) state 0, STANDBY (0,1) state 1, TEMPORARY state 2, 3V SUSPEND (1,0) state 3, 0-V SUSPEND (1,0) state 4, and OFF (1,1) state 5." While these portions refer to a reduction of *system* power consumption, the instant claim calls for placing the *bus* in a reduced power consumption state. Still, one may argue, reasonably, that if system power consumption is reduced, then any system bus must also be in a reduced power consumption mode, especially in view of Walsh's disclosure of a "bus-quieting" mode.

However, the instant claim does not merely require that the bus be placed in a reduced power consumption state. It requires

that the bus coupling the two integrated circuits have signal lines including a bus clock, a data in signal line and a data out signal line and that the signal lines, including the bus clock, be inactive when the bus is placed in a reduced power consumption state. Moreover, the existence of the wake-up event recited in the preamble of the claim must be signaled "by changing at least one signal line of the bus from a first voltage level to a second voltage level while the bus clock is inactive, in response to the wake-up event detected by the second integrated circuit."

While the examiner points to Walsh, at column 29, lines 49-56, and column 27, line 66 to column 28, line 2, for changing a signal line of the bus from a first voltage to a second voltage in response to a wake-up event recognized by the second integrated circuit, our review of these portions of Walsh does not comport with the examiner's position.

These portions of Walsh relate to the six states of a state machine shown in Figure 23. We find nothing therein, and the examiner has not convincingly pointed to anything therein, that relates to the bus 104 having a bus clock, and data in and data out signal lines wherein the signal lines and the clock are inactive when the bus is placed in a reduced power consumption state and wherein the existence of a wake-up event is signaled

"by changing at least one signal line of the bus from a first voltage level to a second voltage level while the bus clock is inactive, in response to the wake-up event detected by the second integrated circuit."

The examiner explains that this is an "inherent" feature of Walsh [answer-page 10] because a "wakeup line would trigger the bus to switch back to a normal operation mode." But Walsh does not even show that the bus has a clock and data in and data out signal lines and that both signal lines and the clock are inactive when the bus is placed in a reduced power consumption state. The examiner surmises [answer-page 10] that Figure 5 of Walsh shows a bus containing a series of signal lines and that "if the bus 104 is placed in the reduced power consumption state such as idle state or sleep state or off state," then "some" of those signal lines will be inactive and "some will be remained active." Thus, even the examiner seems to admit that it is unclear which, if any, of the bus signal lines will be inactive during a reduced power consumption state. It is improper to base an anticipation rejection under 35 U.S.C. 102 on speculation.

Accordingly, appellant has made a reasonable argument that "Walsh fails to teach utilizing a signal line of a bus to signal existence of a wake-up event and changing the bus to a normal

power consumption state in response to a change in voltage on that signal line" [brief-page 4] and, in our view, the examiner has not successfully rebutted that argument.

Thus, we will not sustain the rejection of claims 1-11 and 21-23 under 35 U.S.C. 102(e).

Turning to independent claim 12, this claim requires, inter alia, that the second bus interface circuit is "responsive to a wake-up event to change the signal line on the bus driven by the second integrated circuit from a first to a second voltage level, thereby providing a wake-up indication to the first integrated circuit indicating that a wake-up event has occurred." The examiner urges that Walsh discloses this at column 29, line 55 to column 30.

Our review of this section of Walsh does not support the examiner's contention.

As discussed by appellant, at page 8 of the brief, this portion of Walsh discusses how a signal VCCON is generated. This VCCON signal is not part of bus 104 and does not couple to the first integrated circuit 102 or bus bridge 716 (which the examiner indicates to be the first bus interface circuit). Therefore, we agree with appellant that Walsh does not appear to teach a second bus interface circuit responsive to a wake-up

event to change the signal line on the bus to provide a wake-up indication.

The examiner's response, at the penultimate page of the answer, is that the second bus interface circuit is an "inherent" feature because "it is understood that the interface circuit is essential for connecting devices together." The examiner's response to just about every argued claim limitation is that it is "inherent" [see the penultimate page of the answer and the preceding page]. The examiner cannot merely assert "inherency" without a convincing explanation as to why such feature is inherent. In order for something to be "inherent", the claimed limitation must necessarily follow from what is taught by the applied reference. There is no indication in Walsh that the interface circuit necessarily operates in the claimed manner or that the entire bus in Walsh is necessarily inactive. Moreover, even assuming, arguendo, that a second bus interface could be considered "inherent," that, in and of itself, does not explain why such a second bus interface would need to be responsive to a wake-up event to change the signal line on the bus driven by the second integrated circuit from a first to a second voltage level, thereby providing a wake-up indication to the first integrated circuit indicating that a wake-up event has occurred.

Accordingly, we will not sustain the rejection of claims 12-19 under 35 U.S.C. 102(e).

Finally, we turn to independent claim 25. This claim also requires a communication of the existence of a wake-up event detected by the second integrated circuit to the first integrated circuit but does so by changing a second unidirectional data line from a first to a second voltage level while the remaining signal lines, including the clock line, are maintained in the power savings mode. Therefore, the bus clock is not in an operating mode at this time. The clock is then restarted "in response to the changing of second unidirectional data line from the first to the second voltage."

We agree with appellant that Walsh does not teach using one of the signal lines of bus 104 to indicate a wake-up event while the clock line on bus 104 is in a power savings mode and then restarting the clock in response to the wake-up indication. Further there are no unidirectional data lines indicated in bus 104 by Walsh. The examiner's rejection indicates that Walsh teaches such unidirectional data lines but the examiner never specifically identifies such lines and we are unaware of such unidirectional lines in Walsh. Further, in response to

appellant's arguments, the examiner offers no rebuttal in the response section of the answer. Accordingly, we also will not sustain the rejection of claims 25 and 26 under 35 U.S.C. 102(e).

The examiner's decision rejecting claims 1-19, 21-23, 25 and 26 under 35 U.S.C. 102(e) is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)	

EK/RWK

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