

The opinion in support of the decision being entered today  
was not written for publication in a law journal  
and is not binding precedent of the Board.

Paper No. 11

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte XIA DAI

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Appeal No. 2001-0184  
Application No. 09/002,173

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BRIEF

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Before THOMAS, KRASS, and BARRETT, Administrative Patent Judges.  
KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of  
claims 1-11, all of the pending claims.

The invention is directed to a method and apparatus for  
binary addition. More particularly, the invention seeks to make  
adder latency independent of the adder width N. The adder

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calculates an N bit sum from an N bit augend and an N bit addend wherein a first circuit speculatively calculates bit N-1 of the sum based only on bit N-1 of the augend, bit N-1 of the addend, and a limited carry bit. The adder also comprises a second circuit for calculating the limited carry bit based only on K bits of the augend and K bits of the addend, where K is less than N-1. A third circuit detects a potential difference between the limited carry bit and an unlimited carry bit.

Representative independent claim 1 is reproduced as follows:

1. An adder having an adder width N, for calculating an N bit sum S from an N bit augend A and an N bit addend B, said adder comprising:

a first circuit for speculatively calculating bit  $S_{N-1}$  based only on bit  $A_{N-1}$ , bit  $B_{N-1}$ , and a limited carry bit;

a second circuit for calculating said limited carry bit based only on K bits of said augend and K bits of said addend, wherein K is less than N-1;and

a third circuit for detecting a potential difference between said limited carry bit and an unlimited carry bit

wherein the adder latency is related to the number of bits, K, in the second circuit;

so that the adder latency is independent of the adder width N.

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The examiner relies on the following reference:

Tomoji                      4,761,760                      Aug. 2, 1988

Claims 1-7 and 9-11 stand rejected under 35 U.S.C. § 102(b) as anticipated by Tomoji.

Claim 8 stands rejected under 35 U.S.C. § 103 as unpatentable over Tomoji.

Reference is made to the brief and answer for the respective positions of appellant and the examiner.

OPINION

At the outset, we note that, in accordance with the grouping of claims at page 3 of the brief, all claims will stand or fall together. Accordingly, we will focus on independent claim 1.

It is the examiner's position that Tomoji's adder 1, which calculates an N bit sum S from an N bit augend SX and an N bit addend SY, comprises a first circuit (elements 304, 308, 318,

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322, 332, 336 and 340 of Figure 2 in the last bit slice block 400) for speculatively calculating bit  $S_{N-1}$  (output of gate 340 of block 400) based only on bit  $SX_{N-1}$ ,  $SY_{N-1}$  and a limited carry bit, presuming that the carry in the arithmetic circuit 224 would be 1; a second circuit (providing the limit carry to gates 332 and 336) for calculating the limited carry bit based only on the next lower K bits of the addend and K bits of the augend; and a third circuit (113 in block 300) for detecting a potential difference between the limited carry bit and an unlimited carry bit, as claimed.

The examiner contends that the latency of the adder 1 for generating the speculative sum (the output of arithmetic circuits 121-124) is clearly related to the number of K bits in each block (Figure 2), but it is independent of the number of bits of the adder because the adder blocks have the same structure and the speculative sum bits generated in each block is clearly independent of the other block.

Appellant's position is that Tomoji "always applies a suspense carry bit to the arithmetic circuit 12j, 'regardless of the generator of the carry bit C1 in the carry lookahead

circuit'" [brief-page 4]. Thus, appellant contends that the arithmetic circuit 12j calculates the sum assuming there is no carry, then the correction circuit 14j corrects the calculated sum if there is a carry so that Tomoji produces a tentative result that is corrected if there is no carry bit.

Appellant argues that Tomoji does not speculatively calculate the bits N-K above a number K so that the adder latency is independent of the adder width. Thus, concludes appellant, the latency of the arithmetic circuit 12j is dependent on the arithmetic circuit width, which is the number of bits added by the arithmetic circuit 12j. "Tomiiji [sic, Tomoji] does not disclose an adder with a latency that is independent of adder width" [brief-page 5].

While the examiner agrees that the instant *disclosed* invention differs from that of Tomoji in the feature that the limited carry bit for each bitslice is generated, in the instant invention, based only on the same number of K preceding bits, it is the examiner's position that this feature is not recited in the instant claims and that the claims only require that the limited carry bit for the most significant bit N-1 is calculated

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based only on K preceding bits but do not limit how the carry bits for the other bitslices are generated. That being the case, the examiner finds that Tomoji shows the broadly claimed subject matter in Figures 1 and 2 for the reasons supra.

We agree with the examiner that the broad language of instant claim 1 does not require the limited carry bit to be generated based only on the same number of K preceding bits and we agree with the examiner that the claim only requires that the limited carry bit for the most significant bit N-1 is to be calculated based only on K preceding bits but does not limit how the carry bits for the other bitslices are generated. Clearly, Tomoji discloses a "first circuit," as claimed, since a bit  $S_{N-1}$  is speculatively calculated by adder 400 based only on bit  $A_{N-1}$  ( $SX_4$ ), bit  $B_{N-1}$  ( $SY_4$ ) and a limited carry bit (suspense carry  $CS_4$ ).

However, we fail to find, in Tomoji, the claimed "second circuit" for calculating the limited carry bit based only on K bits of said augend and K bits of said addend, wherein K is less than N-1. This is so because the suspense carry bit (i.e., the "limited carry bit") is not calculated at all but, rather, it is preset to either a 1 or a 0 and this suspense carry bit is always

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applied "regardless of the generation of the carry bit  $C_i$  in the carry lookahead circuit on its right" [column 3, lines 15-16, of Tomoji].

The examiner argues that this second circuit is disclosed by Tomoji by "the corresponding circuit that provide [sic, provides] the limited carry to gates 332 and 336" [answer-page 4]. However, whatever is providing this limited carry in Tomoji *always* supplies the same suspense carry bit and so it is not "based only on  $K$  bits of said augend and  $K$  bits of said addend...", as claimed.

Accordingly, since an important claim limitation is absent from the teachings of Tomoji, Tomoji cannot anticipate the claimed subject matter and we will not sustain the rejection of claims 1-7 and 9-11 under 35 U.S.C. 102(b).

Similarly, since we find no reason to modify Tomoji to provide for this deficiency, we also will not sustain the rejection of claim 8 under 35 U.S.C. § 103.

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The examiner's decision is reversed.

REVERSED

JAMES D. THOMAS	)	
Administrative Patent Judge	)	
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	)	
ERROL A. KRASS	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
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	)	
LEE E. BARRETT	)	
Administrative Patent Judge	)	

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