

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte IN-HO CHA and BYOUNG-KWON PARK

Appeal No. 2000-2188
Application No. 09/063,050¹

HEARD: APRIL 10, 2002

Before RUGGIERO, DIXON and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1 through 10, which are all of the claims pending in this application.

BACKGROUND

Appellants' invention is directed to a boosted voltage generator that decreases power consumption by adjusting the bandwidth of the clock signal proportional to that of the load

¹ Application for patent filed April 21, 1998, which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Korean Application 14714/1997, filed April 21, 1997.

drive current. According to Appellants, conventional boosted-voltage generators operate based on an internal oscillator that generates the clock signal. Since the internal oscillator has a fixed frequency, its band width is limited, which results in a higher level of load drive current and increased power consumption (specification, page 4). To resolve the limitations of internal oscillator, an externally applied clock signal is received by a pump controller in the voltage generator (specification, page 7). Thus, according to Appellants, as the period of the clock signal decreases (increases), the current consumed by the load becomes larger (smaller) (specification, page 7).

Representative independent claim 1 is reproduced as follows:

1. A synchronized boosted voltage generator, comprising:

a first means for receiving an externally applied clock signal and an externally applied control signal, and outputting first, second and third signals;

a charging means for receiving the first signal and charging a node;

a second means for receiving the second signal and clamping a potential on the node so as not to fall below a predetermined voltage;

a third means for receiving the third signal and outputting a fourth signal which is to control a pumping operation;

been withdrawn by the Examiner. See Ex parte Emm, 118 USPQ 180, 181 (Bd. App. 1957).

Rather than reiterate the conflicting viewpoints advanced by the Examiner and Appellants regarding the above-noted rejections, we make reference to the answer (Paper No. 13, mailed June 6, 2000) for the Examiner's complete reasoning, the appeal brief (Paper No. 12, filed March 31, 2000) and the reply brief (Paper No. 14, filed August 7, 2000) for Appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to Appellants' specification and claims, to the applied prior art reference, and to the respective positions articulated by Appellants and the Examiner. As a consequence of a careful review of the evidence before us, we disagree with the Examiner that claims 7 and 8 are properly rejected under the second paragraph of 35 U.S.C. § 112. However, it is our view that the admitted prior art anticipates the subject matter of claims 1 and 4. We are also of the view that the admitted prior art and Gazda would have not suggested the subject matter of claims 2, 3 and 5 through 10. Accordingly, we affirm-in-part.

With respect to the rejection of claims 7 and 8 under the second paragraph of 35 U.S.C. § 112, Appellants argue that the claims require an externally applied clock signal supplied from a "clock signal generator" (brief, pages 5 & 6). Appellants further point out that the relationship between the clock signal generator and the voltage generator is apparent as the claims recite that the "externally applied clock signal is received from a clock signal generator" and "communicates with the voltage generator" (brief, page 6). Appellants also rely on Figures 4 and 7 to assert that the "externally applied clock signal" comes from outside the depicted circuit (brief, page 8 and reply brief, page 3).

In response, the Examiner indicates that the externally applied clock signal of claim 7 is interpreted as "the output of the clock signal generator [that is] being related to the output of the voltage generator." The Examiner concludes that the clock signal is not an externally applied signal and cannot communicate with the voltage generator (answer, page 5).

Analysis of a rejection under 35 U.S.C. § 112, second paragraph, should begin with the determination of whether claims set out and circumscribe the particular area with a reasonable degree of precision and particularity; it is here where

definiteness of the language must be analyzed, not in a vacuum, but always in light of teachings of the disclosure as it would be interpreted by one possessing ordinary skill in the art. In re Johnson, 558 F.2d 1008, 1015, 194 USPQ 187, 193 (CCPA 1977), citing In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (1971). "The legal standard for definiteness is whether a claim reasonably apprises those of skill in the art of its scope." In re Warmerdam, 33 F.3d 1354, 1361, 31 USPQ2d 1754, 1759 (Fed. Cir. 1994). Furthermore, our reviewing court points out that a claim which is of such breadth that it reads on subject matter disclosed in the prior art is rejected under 35 U.S.C. § 102 rather than under 35 U.S.C. § 112, second paragraph. See In re Hyatt, 708 F.2d 712, 715, 218 USPQ 195, 197 (Fed. Cir. 1983) citing In re Borkowski, 422 F.2d 904, 909, 164 USPQ 642, 645-46 (CCPA 1970).

Upon a careful review of the claim language and the specification, we find that the claimed limitation of "the externally applied clock signal is received from a clock signal generator that communicates with the voltage generator" refers to a clock signal generator that sends the clock signal to the voltage generator. It is clear from the specification as a whole and page 8, lines 27-31 and page 9, lines 8-12 specifically, that

the clock signal may be generated by a clock signal generator such as a "synchronous semiconductor" that provides its signal to (communicates with) the claimed synchronized boosted voltage generator.

In view of the above and in light of the specification as a whole, we find that the externally applied clock signal received from a clock signal generator communicating with the voltage generator is sufficiently defined and would reasonably apprise those skilled in the art of the scope of this limitation. Accordingly, we will not sustain the rejection of claims 7 and 8 under the second paragraph of 35 U.S.C. § 112.

Turning to the 35 U.S.C. § 102 rejection of claims 1 and 4, we note that the focus of Appellants' arguments is that the admitted prior art does not disclose or suggest the claimed "externally applied clock signal" since the signal is derived from internal oscillator 10 (oral hearing, brief, page 8 and reply brief, page 4). Appellants further point out that the signal OSC is generated by the internal oscillator which is part of and internal to the voltage generator of Figure 1. Appellants argue that the output of an internal oscillator is not a clock signal that is externally applied (oral hearing and brief, page 9). Appellants further argue that the Examiner did not make the

necessary findings related to the functions specified in claim 1, i.e., receiving an externally applied clock signal, and chose a different function (brief, page 9). Additionally, Appellants point out that although claim 4 does not fall under paragraph 6 of § 112, its functional limitations cannot be ignored (brief, page 10).

In response to Appellants' arguments, the Examiner asserts that the signal OSC is an external signal with respect to the voltage generator since the signal is produced independent of the voltage generator (answer, page 6). The Examiner further reasons that although the oscillator and the voltage generator may be formed on a single chip, the signal OSC comes from "somewhere" external with respect to the voltage generator circuit and is externally applied to the pump controller (answer, page 6).

Before addressing the Examiner's rejection based upon prior art, it is essential that we understand the claimed subject matter and determine its scope. Claim interpretation must begin with the language of the claim itself. See Smithkline Diagnosics, Inc. v. Helena Laboratories Corp., 859 F.2d 878, 882, 8 USPQ2d 1468, 1472 (Fed. Cir. 1988). Accordingly, as required by our reviewing court, we will initially direct our attention to Appellants' claim 1 in order to determine its scope.

"[T]he name of the game is the claim." In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). Claims will be given their broadest reasonable interpretation consistent with the specification, and limitations appearing in the specification are not to be read into the claims. In re Etter, 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985).

Appellants' claim 1 requires "a first means for receiving an externally applied clock signal" and an "externally applied control signal" wherein "first, second and third signals" are outputted by the first means. We find that the "a first means for receiving" limitation is in means-plus-function format. The term "means" in this limitation creates a presumption that a section 112, ¶ 6 interpretation is called for. In construing a means-plus-function limitation, we must identify both the claimed function and the corresponding structure in the written description for performing that function. Under § 112, ¶ 6, functional limitations that are not recited in the claim, or structural limitations from the written description that are unnecessary to perform the claimed function may not be imported into the claims. Micro Chem., Inc. v. Great Plains Chem. Co., 194 F.3d 1250, 1258, 52 USPQ2d 1258, 1263 (Fed. Cir. 1999);

citing Rodime PLC v. Seagate tech., Inc., 174 F.3d 1294, 1302, 50 USPQ2d 1429, 1435 (Fed. Cir. 1999).

After reviewing the specification, we find that the claimed first means corresponds to pump controller 20 (identical elements in Figures 1 and 4). The claimed voltage generator includes a pump controller that receives an externally applied clock signal and an externally applied control signal (specification, page 6, lines 13-17). However, the specification refers to the clock signal merely as "externally applied clock signal" without specifying the source of the signal or what element the signal is external to (specification, pages 6 & 7). At the best, a "synchronous semiconductor" is mentioned in the specification without identifying its relation with respect to the voltage generator (specification, pages 8 & 9). Moreover, based on Appellants' own disclosure and lack of any further description for the term "externally," we see no reason to interpret the term "externally applied" in any way other than its common meaning, i.e., applied from outside of the pump controller. See Cortland Line Co. v. Orvis Co., 203 F.3d 1351, 1356, 53 USPQ2d 1734, 1737 (Fed. Cir. 2000) ("[c]laim terms receive their ordinary and customary meaning unless the patentee assigns a special meaning.") (citing Vitronics Corp. v. Conceptronic, Inc., 90 F.3d

1576, 1582, 39 USPQ2d 1573, 1576 (Fed. Cir. 1996)). In the present case, absent any specified external source of clock signal, "an externally applied clock signal" is a signal that is merely external to the first means.

With respect to Appellants' claim 4, we also find that the claim requires a voltage generator comprising a pump controller that receives "an externally applied clock signal" and an "externally applied control signal." The pump controller then outputs "first, second and third signals." As discussed above with respect to claim 1, we conclude that "an externally applied clock signal" is a signal that is required to be external with respect to only the pump controller.

A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. See Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999); In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994). Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital

Data Sys. Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

After reviewing the description of the admitted prior art and in view of our analysis above, we agree with the Examiner that "a first means for receiving an externally applied clock signal" reads on pump controller 20 of Figure 1. The "externally applied clock signal" reads on signal OSC in Figure 1 which is externally applied to a pump controller and is outputted by the oscillator, which in turn, constitutes a source that is external to the pump controller. We further find that the prior art voltage generator of Figure 1 includes an internal oscillator outputting an internal oscillation signal OSC and a pump controller that receives the internal oscillation signal and an external control signal (specification, page 1, lines 11-15). Although the source of the oscillation signal is defined as being internal to and a part of the voltage generator, the oscillator is external to the pump controller and its OSC output signal is generated outside the pump controller.

In view of our analysis above, we find that the prior art of Figure 1 discloses all the limitations of Appellants' claims 1 and 4. We are further unpersuaded by Appellants' assertion that the Examiner incorrectly equated an output of an oscillator with

a clock signal. We note that signal OSC generated by the oscillator (as depicted in Figure 2A) has the same properties of the claimed clock signal (as depicted in Figure 5A) since clock pulses are basically pulses generated by an oscillator.³

Therefore, the Examiner has met the burden of providing a prima facie case of anticipation. Accordingly, the rejection of claims 1 and 4 under 35 U.S.C. § 102 over the admitted prior art in Figure 1 is sustained.

We next consider the Examiner's 35 U.S.C. § 103 rejection of claims 2, 3 and 5 through 10 based upon the combination of the prior art of Figure 1 and Gazda. Appellants argue that Gazda fails to provide any teachings or suggestions for modifying the prior art of Figure 1 to overcome the deficiencies discussed above. Appellants further point out that there is no suggestion in any of the references for the Examiner's proposed combination (brief, page 12 and reply brief, page 6). Finally, Appellants argue that the limitation of "variable dynamic range," as recited in claims 9 and 10, is not taught by any of the references (brief, page 11 and reply brief, page 5).

³ Microsoft Press Dictionary, 2nd edition , 1994, pp. 76, 283 (copy of which accompanies this decision).

The Examiner's rejection is based on modifying the voltage generator of the prior art with the frequency divider of Gazda "to achieve a desired frequency if the input frequency is not within the desired value or range" (answer, page 4). In response to Appellants' arguments, the Examiner asserts that expanding the spectrum of an oscillator by adding a frequency divider is "normal practice for one skilled in the art" (answer, page 7). The Examiner further argues that the "variable dynamic range," as recited in claims 9 and 10, is a well-known characteristic of clock signals (answer, page 8).

The initial burden of establishing reasons for unpatentability rests on the examiner. In re Oetiker, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). Where, as here, a conclusion of obviousness is premised upon a combination of references, the examiner must identify a reason, suggestion, or motivation which would have led an inventor to combine those references. Pro-Mold & Tool Co. V. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1629, (Fed. Cir. 1996). However, "the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support

the agency's conclusion." In re Lee, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

A review of Gazda and Appellants' prior art of Figure 1 reveals no teaching related to a clock signal generator that communicates with the voltage generator, as recited in claims 7 and 8, dependent upon claims 1 and 4 respectively. We further find that the Examiner has failed to provide evidence in support of "variable dynamic range," as recited in claims 9 and 10, being a well-known characteristic of clock signals and obvious to one of ordinary skill in the art. With respect to the features of claims 2 and 5, as well as claims 3 and 6 which are dependent thereupon, requiring a frequency divider for outputting an internal clock signal applied to the pump controller, we note that Gazda merely uses programmable divider circuits in an oscillator. The fixed frequency divider of Gazda is replaced with a programmable one in order to expand the frequency range of a voltage controlled crystal oscillator (col. 4, lines 24-33).

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir.

1992), citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). The court finds it "impermissible to use the claims as a frame and the prior art references as a mosaic to piece together a facsimile of the claimed invention." Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988), citing W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 220 USPQ 303, 312 (Fed. Cir. 1983).

Upon our review of Gazda, we find that Gazda teaches an oscillator with extended frequency range using frequency dividers. However, we fail to find any teaching or suggestion to use frequency dividers in a voltage generator for dividing the frequency of the clock signal. Furthermore, we fail to find any teaching or suggestion for providing a clock signal generated by a clock signal generator that communicates with the voltage generator. Thus, we find no support for the Examiner's conclusion that modifying the prior art of Figure 1 with the teachings of Gazda would have suggested Appellants' claimed clock signal generator having a frequency divider or a clock signal with a variable dynamic range. Accordingly, we do not sustain the 35 U.S.C. § 103 rejection of claims 2, 3 and 5 through 10 over Appellants' prior art of Figure 1 and Gazda.

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 7 and 8 under the second paragraph of 35 U.S.C. § 112 is reversed. The decision of the Examiner rejecting claims 1 and 4 under 35 U.S.C. § 102 is affirmed. The decision of the Examiner rejecting claims 2, 3 and 5 through 10 under 35 U.S.C. § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JOSEPH F. RUGGIERO)
Administrative Patent Judge)
)
)
)
)
) BOARD OF PATENT
JOSEPH L. DIXON) APPEALS
Administrative Patent Judge) AND
) INTERFERENCES
)
)
)
MAHSHID D. SAADAT)
Administrative Patent Judge)

Appeal No. 2000-2188
Application No. 09/063,050

Page 18

Birch, Stewart, Kolasch & Birch
P. O. Box 747
Falls Church, VA 22040-0747