

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PO-CHIH WANG, CHUNG-YI YAO,
THOMAS SHENG and YEN-CHENG CHEN

Appeal No. 2000-2067
Application No. 08/859,278

ON BRIEF

Before FLEMING, RUGGIERO and GROSS, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge.***

Decision on Appeal

This is a decision on appeal from the final rejection of claims 1 through 23, all the claims pending in the application.

The invention relates to an image processing system. The system includes a central processing unit, CPU, (604) to control the scanning of the scanner (602) and the transmission of the scanned information. See Appellants' specification page 8, lines 4-10. The system further includes a second processor, an image processor (603/701). See Appellants' specification page 8, lines 13-17, page 9, lines 10-14 and Figures 6 and 7. The image processor (603/701) is for processing the scanned information in

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terms of features from a group consisting of scaling (702), density control (703), background detection (703), edge detection (704) and error diffusion (706). See Appellants' specification pages 9-11, and Figure 7.

Independent claim 1 present in the application is reproduced as follows:

1. An image processing system to receive and process scanned information from a scanner, comprising:

a central processing unit to control the scanning of said scanner and the transmission of said scanned information,

an image processor dedicated to process said scanned image information in terms of features from a group consisting of scaling, density control, background detection, edge detection, error diffusion,

an image storage device connected only to said image processor to store any pre-processed and processed image information,

wherein said pre-processed and said processed image information can be selected between storing in a computer and sending to a printer for printout.

References

The references relied on by the Examiner are as follows:

Enoki et al. (Enoki)	4,885,223	Dec. 05, 1989
Miller et al. (Miller)	5,014,333	May 07, 1991
Kawamata et al. (Kawamata)	4,989,163	Jan. 29, 1991

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Hirota	5,177,623	Jan. 05, 1993
Cohen-Skalli et al. (Cohen-Skalli)	5,235,674	Aug. 10, 1993
Kajitani et al. (Kajitani)	5,572,337	Nov. 05, 1996

Rejections at Issue

Claims 1, 2, 4, 7 through 17 and 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cohen-Skalli, Kawamata and Hirota. Claims 3 and 6 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cohen-Skalli, Kawamata, Hirota, Miller and Kajitani. Claim 5 stands rejected under 35 U.S.C. § 103 as being unpatentable over Cohen-Skalli, Kawamata, Hirota and Enoki. Claims 18, 19, 21 and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cohen-Skalli and Hirota. Claim 23 stands rejected under 35 U.S.C. § 103 as being unpatentable over Cohen-Skalli and Kawamata.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief¹ and the Answer for the respective details thereof.

¹ Appellants filed an Appeal Brief on March 17, 2000. In response to an order for compliance, Appellants filed a supplement to the Appeal Brief on February 21, 2002.

OPINION

After a careful review of the evidence before us, we do not agree with the Examiner that claims 1 through 23 are unpatentable under 35 U.S.C. § 103.

First we will address the rejection of claims 1, 2, 4, 7 through 12 as being unpatentable under 35 U.S.C. § 103 over Cohen-Skalli, Kawamata and Hirota. We note that Claim 1 is the independent claim with claims 2, 4 and 7 through 12 dependent on claim 1.

Appellants argue that "Cohen-Skalli's processing unit 13 is not an image processing unit in the sense that it does not perform image processing functions." See page 2, lines 26-27 of the Brief. Appellants then argue that "[t]he Cohen-Skalli's processing unit 13 performs other functions than controlling the signal flow of the image signal." See page 2, lines 29 to page 3, line 1 of the Brief. Appellants further argue that a separate image processor is used in the system because "[t]he design and cost of separate Image Processor and a main CPU are less than combining all the functions in one single CPU." See page 3, lines 9-10 of the Brief.

For the rejection of claim 1, the Examiner states that,

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Cohen-Skalli et al discloses an image processing system (10) to receive and process scanned information from a scanner (8), comprising: **a central processing unit (13) to control the transmission of the scanned information; an image processor (13) dedicated to process the scanned image information according to a mode selected by a user**

(Emphasis added). See page 11, lines 5-10 of the Answer.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Further, our reviewing court in *In re Dembiczak*, 175 F.3d 994, 999-00, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) has said,

Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence.' *E.g.*, *McElmurry v. Arkansas Power & Light Co.*, 995 F.2d 1576, 1578, 27 USPQ2d 1129, 1131 (Fed. Cir. 1993) ("Mere denials and conclusory statements, however, are not sufficient to establish a genuine issue of material fact."); *In re Sichert*, 566 F.2d 1154, 1164, 196 USPQ 209, 217 (CCPA 1977).

We note that the Appellants' claim 1 recites the following:

a central processing unit to control the scanning of said scanner and the transmission of said scanned information;

an image processor dedicated to process said scanned information

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(Emphasis added). In understanding these claim limitations, we identify the separate hardware components of an independent central processing unit and an independent image processor. Figure 6 clearly shows the separate hardware of an image processor (603) and a CPU (604), each with separate functions and connections to various components of the image processing system (601). Figure 7 further illustrates the independence and functionality of the image processor (701 - which is the same component as 603). We find that Appellants' claim calls for two separate processors. We cannot agree that a "single CPU" with software that makes the CPU function in two processing modes is the same as two distinct processors.

Upon careful review of Cohen-Skalli, we find that Cohen-Skalli discloses "[a] processing and computing unit 13 connected to a control panel 18 has the function of controlling the storage unit 12, the routing unit 14 and the series interfaces 19.1, 19.2, 19.N." See column 3, line 68 to column 4, line 4 and Figures 1 and 2 of Cohen-Skalli. Cohen-Skalli further discloses that "the routing unit 14 transmits the data either solely to the storage unit 12 for printing or also to the other series ports (19.1, 19.2, 19.3, 19.N) concerned for data-processing in one or a number of external microcomputers (7.1, 7.2, 7.N)." See column

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4, lines 60-65 of Cohen-Skalli. Cohen-Skalli also discloses that the routing unit (14) is connected to an encoding unit (15.2). See column 3, lines 59-62 of Cohen-Skalli. Further disclosed by Cohen-Skalli is a scanner 8 connected to the routing unit (14) via an interface (20). See column 3, lines 49-58 of Cohen-Skalli. Upon reviewing Cohen-Skalli, we find nothing in the reference that teaches two different processors, (*i.e.*, a central processing unit and an image processor) for processing in an image processing system.

We fail to find anywhere in the Answer where the Examiner has provided arguments or suggestions to modify the single CPU arrangement disclosed by Cohen-Skalli to be a dual processor system as claimed. Rather, as stated *supra*, we find that the Examiner relies on the processor (13) to do both the central processing and the image processing. Further, having reviewed the remaining references, Kawamata and Hirota, we fail to find factual basis or motivation for suggesting the modification of the single CPU arrangement disclosed by Cohen-Skalli to be a dual processor system as claimed. Instead, we note that these references are relied upon by the Examiner to meet alternative claim limitations and we find that these references disclose image processing systems with single processors. Therefore, we

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will not sustain the Examiner's rejection of claim 1. Further, Claims 2, 4 and 7 through 12 are dependent on claim 1, and therefore include the aforementioned limitations of claim 1. Therefore, we will not sustain the Examiner's rejection of claims 2, 4 and 7 through 12 for the same reasons as above. We also note that the remaining independent claims, claims 13, 18 and 23, require the limitations of two independent processors as discussed with respect to claim 1. Since the Examiner again relied on the Cohen-Skalli reference for teaching the limitations of two independent processors, for the reasons set forth *supra*, we will not sustain the Examiner's rejection of claims 13, 18 and 23. Lastly, we will not sustain the rejection of claims 14 through 17 and 19 through 22, which are dependent on claims 13 and 18 and therefore include the aforementioned limitations of claims 13 and 18.

We note that in rejecting claims 3 and 6 under 35 U.S.C. § 103, which are dependent on independent claim 1, the Examiner further applied the Kajitani and Miller references to the combination of the Cohen-Skalli, Kawamata and Hirota references. However, we find nothing in the Kajitani and Miller references that provides any suggestion for overcoming the Cohen-Skalli, Kawamata and Hirota references' deficiency of failing to teach

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the claimed separate processors found in claim 1 and thereby included in the limitations of claims 3 and 6. Therefore, we will not sustain the Examiner's rejection of claims 3 and 6.

We also note that in rejecting claim 5 under 35 U.S.C. § 103, which is dependent on independent claim 1, the Examiner further applied the Enoki reference to the combination of the Cohen-Skalli, Kawamata and Hirota references. However, we find nothing in the Enoki reference that provides any suggestion for overcoming the Cohen-Skalli, Kawamata and Hirota references' deficiency of failing to teach the claimed separate processors found in claim 1 and thereby included in the limitations of claim 5. Therefore, we will not sustain the Examiner's rejection of claim 5.

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In view of the foregoing, the decision of the examiner
rejecting claims 1 through 23 under 35 U.S.C. § 103 is reversed.

REVERSED

MICHAEL R. FLEMING)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
)	
ANITA PELLMAN GROSS)	
Administrative Patent Judge)	

MRF/sld

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HUNG CHANG LIN
8 SCHINDLER COURT
SILVER SPRING, MD 20903

SHEREECE DAVIS

Appeal No. 2000-2067
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APJ FLEMING

APJ RUGGERIO

APJ GROSS

DECISION: REVERSED

Prepared: July 22, 2003