

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GREGORY J. MANLOVE, MARK B. KEARNEY,
RICHARD J. RAVAS, and RICHARD J. RAVAS

Appeal No. 2000-0312
Application No. 08/610,007

ON BRIEF

Before HAIRSTON, FLEMING, and DIXON, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 22.

The disclosed invention relates to a circuit for compensating for variations in a dc offset component of an input ac signal.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. Analog signal conditioning circuitry comprising:

an amplifier having a first input receiving an analog input signal defined by a first ac signal component due to a driving force and a first dc offset component independent of the driving force, a second input receiving a reference signal and an output providing an analog output signal defined by an amplified representation of the analog input signal and said reference signal; and

a feedback circuit having a periodic clock signal associated therewith, a first input coupled to said amplifier output, a second input receiving said reference signal, and an output connected to said first input of said amplifier for providing an analog feedback signal thereto, said feedback circuit incrementally increasing said analog feedback signal each clock cycle that said analog output signal exceeds said reference signal and incrementally decreasing said analog feedback signal each clock cycle that said reference signal exceeds said analog output signal, said analog feedback signal compensating for variations in said first dc offset component of said analog input signal to thereby maintain the amplified representation of said first dc offset component of said analog output signal within a predefined range of said reference signal.

The reference relied on by the examiner is:

Masuda	4,356,450	Oct. 26,
		1982

Claims 1 through 6, 8 through 14 and 16 through 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Masuda.

Appeal No. 2000-0312
Application No. 08/610,007

Claims 1 through 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the admitted prior art circuit of Figure 1 in view of Masuda.

OPINION

We have carefully considered the entire record before us, and we will reverse all of the rejections of record.

Masuda discloses a circuit (Figure 3) that compensates for an offset voltage that arises in an operational amplifier 22. A feedback circuit connected between the output and the input of the operational amplifier 22 includes a comparator 28, a pulse signal generating circuit 40, an AND gate 30, an U/D counter 44, a D/A converter 50, and a voltage to current converter 52. The examiner acknowledges (answer, page 3) that Masuda "does not disclose that the inverting input of the amplifier 22 receives an input signal comprising an AC component and a DC component as called for in claim 1." Notwithstanding this deficiency in the

Appeal No. 2000-0312
Application No. 08/610,007

teachings of Masuda, the examiner is of the opinion (answer, page 4) that:

Those having ordinary skill in the art would recognize that the DC offset circuit of Masuda also can be used to compensate for DC offset voltage on the input signal 10 by connecting the non-inverting terminal and the inverting terminals of the amplifiers (22, 28) to predetermined reference voltages. Thus, compensating DC offset voltage on the input signal of the Masuda circuit is a routine design expedient for an engineer depending upon the particular environment and the applications in which the Masuda circuit is to be used.

The examiner's contentions to the contrary notwithstanding, Masuda never indicates that there is a dc offset voltage on the input signal 10. In Masuda, either a dc offset voltage (i.e., a reference voltage at ground potential) or an input signal 10 is provided as an input to amplifier 22 via two-position switch 14. The input to amplifier 22 never simultaneously receives both the reference voltage and the input signal. Accordingly, we agree with the appellants' argument (reply brief, page 3) that "it would be impossible with this circuit configuration to 'compensate for variations in a dc offset component of an analog input signal' as required by Applicants' claimed invention." We also agree with appellants' arguments (reply brief, page 4) that "in the Masuda reference, the dc offset voltage being

compensated . . . is a dc offset voltage internal to amplifier (22)," and that the feedback circuit in Masuda does not increment and decrement the feedback signal in the manner required by the claimed invention. In short, we agree with the appellants' argument (reply brief, page 6) that the examiner has resorted to impermissible hindsight to demonstrate the obviousness of the claimed invention based upon the teachings and suggestions of Masuda. Based upon the foregoing, the 35 U.S.C. § 103(a) rejection of claims 1 through 6, 8 through 14 and 16 through 22 based upon Masuda alone is reversed.

Turning lastly to the obviousness rejection of claims 1 through 22 based upon the combined teachings of appellants' admitted prior art Figure 1 and Masuda, we agree with the examiner's observation (answer, page 4) that the processing circuit in Figure 1 of Masuda does not disclose the claimed feedback circuit. As indicated supra, the feedback circuit in Masuda does not function in the manner required by the claims on appeal. Thus, we agree with appellants' argument (brief, page 15) that "[a]pplicants' prior art circuit illustrated in FIG. 1 provides no motivation to a person of ordinary skill in the art to utilize the Masuda feedback circuitry for any other reason

Appeal No. 2000-0312
Application No. 08/610,007

than that disclosed by Masuda; namely to tune an amplifier stage to compensate for a single dc offset value." In summary, the 35 U.S.C. § 103(a) rejection of claims 1 through 22 based upon the admitted prior art and Masuda is reversed.

DECISION

The decision of the examiner rejecting claims 1 through 22 under 35 U.S.C. § 103(a) is reversed.

REVERSED

Appeal No. 2000-0312
Application No. 08/610,007

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	
)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
)	
JOSEPH L. DIXON)	
Administrative Patent Judge)	

KWH/lp

Appeal No. 2000-0312
Application No. 08/610,007

JIMMY FUNKE
DELCO ELECTRONICS CORPORATION
MAIL STOP D32
PO BOX 9005
KOKOMO IN 46904

Letty

JUDGE HAIRSTON

APPEAL NO. 2000-0312

APPLICATION NO. 08/610,007

APJ HAIRSTON

APJ FLEMING

APJ DIXON

DECISION: **REVERSED**

PREPARED: Aug 20, 2002

OB/HD

PALM

ACTS 2

DISK (FOIA)

REPORT

BOOK